

ETX[®] conga-E852/855



Intel[®] Pentium[®]/Celeron[®] M processor with an Intel[®] 852/855 chipset

User's Guide

Revision 0.2 (Preliminary)

Revision History

Revision	Date (dd.mm.yy)	Author	Changes
0.1	03.11.06	GDA	Initial release
0.2	07.12.06	GDA	Updated BIOS description.

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-E852/855. It is one of three documents that should be referred to when designing an ETX[®] application. The other reference documents that should be used include the following:

- ETX[®] Design Guide
- ETX[®] Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

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Intended Audience

This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

Symbols

The following symbols are used in this user's guide:



Warning

Warnings indicate conditions that, if not observed, can cause personal injury.



Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.



Note

Notes call attention to important information that should be observed.

Terminology

Term	Description
GB	Gigabyte (1,073,741,824 bytes)
GHZ	Gigahertz (one billion hertz)
kB	Kilobyte (1024 bytes)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
kHz	Kilohertz (one thousand hertz)
MHz	Megahertz (one million hertz)
T.O.M.	Top of memory = max. DRAM installed
PATA	Parallel ATA
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

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- AMIBIOS8_SerialRedirection.pdf
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ETX[®] Concept

The ETX[®] concept is an off the shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific baseboard. ETX[®] modules have a standardized form factor of just 95mm x 114mm and have identical pinouts on the four system connectors. The ETX[®] module provides most of the functional requirements for any application. These functions include, but are not limited to, graphics, sound, keyboard/mouse, IDE, Ethernet, parallel, serial and USB ports. Four ruggedized connectors provide the baseboard interface and carry all the I/O signals to and from the ETX[®] module.

Baseboard designers can utilize as little or as many of the I/O interfaces as deemed necessary. The baseboard can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly ETX[®] applications are scalable, which means once a product has been created there is the ability to diversify the product range through the use of different performance class ETX[®] modules. Simply unplug one module and replace it with another, no redesign is necessary.

Lead-Free Designs (RoHS)

As of July 2006 all electronic products are required to be environmentally friendly. In future, many of the currently available embedded computer modules will not be offered as lead-free variants. For this reason all congatec AG designs are created from lead-free components and are completely RoHS compliant. This makes congatec AG products ideal lead-free substitutes for new and existing designs.

conga-E852/855 Options Information

The conga-E852/855 is available in five different optional variants. This user's guide describes all of these options. Below you will find an order table showing the different configurations that are currently offered by congatec AG. Check the table for the Part no./Order no. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Part-No.	016029	012347	024714	034712	024172
CPU	Celeron M 600MHz	373 Celeron M 1 GHz	713 Pentium M 1.1GHz	738 Pentium M 1.4GHz	Pentium M 1.6GHz
Cache	512 kByte	512 kByte	1 MByte	2 MByte	1 MByte
Chipset	82852GM	82855GME	82855GME	82855GME	82855GME
DVO	Yes	Yes	Yes	Yes	Yes
USB 2.0	4x	4x	4x	4x	4x

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1 Specifications

1.1 Feature List

Table 1 Feature Summary

Form Factor	ETX [®] standard (Rev. 2.7)
Processor	Intel [®] Celeron [®] M 600MHz ULV with 512-kbyte L2 cache (ultra low voltage) Intel [®] Celeron [®] M 373 1.0GHz with 512-kbyte L2 cache (ultra low voltage) Intel [®] Pentium [®] M 713 1.1GHz with 1-MByte L2 cache (ultra low voltage) Intel [®] Pentium [®] M 738 1.4GHz with 2-MByte L2 cache (low voltage) intel [®] Pentium [®] M 1.6GHz with 1-MByte L2 cache
Memory	SO-DIMM DDR200/266/333 up to 1-GByte (DDR333 only supported on modules with 82855GME chipset)
Chipset	Graphics and Memory Controller Hub Intel [®] 82852GM/82855GME Intel [®] I/O Controller Hub 82801DB (ICH4)
Audio	Realtek ALC 655 AC'97 Rev. 2.2 compatible.
Ethernet	ICH4 with PHY Intel [®] 82562
Graphics Options	Intel [®] Extreme Graphics [®] 3D Video Controller with 64 MByte Dynamic Video Memory Technology (DVMT) and Dual independent display support. <ul style="list-style-type: none"> • CRT Interface 350 MHz RAMDAC Resolutions up to 2048x1536 @ 60Hz (QXGA) including 1920x1080 @ 85Hz (HDTV) • Motion Video Support Hardware motion compensation Subpicture support Dynamic bob and weave • AUX Output Intel compliant DVO 2.0 Port (12Bit DDR) Supports external DVI transmitter with a bandwidth up to 165MHz (UXGA) • Flatpanel Interface 2x112MHz LVDS Transmitter Resolutions up to 1600x1200 Supports all 1x18, 2x18, 1x24, 2x24 Bit TFT configurations (current chipset revisions support 24Bit modes although not officially stated by Intel[®]) Supports both conventional (FPDI) and non-conventional (LDI) color mappings Automatic Panel Detection via EPI (Embedded Panel Interface based on VESA EDID™ 1.3)
Super I/O	Winbond 83627HG
Peripheral Interfaces	<ul style="list-style-type: none"> • PS/2 Keyboard, Mouse • PCI Bus Rev. 2.1 • ISA Bus • 2x EIDE (UDMA-66/100) • 4x USB 2.0 (EHCI) <ul style="list-style-type: none"> • I²C Bus, Fast Mode (400 kHz) • Floppy (shared with LPT) • LPT (EEP/ECP, shared with floppy) • 2 x COM Ports, TTL Level • 1 x IrDA Port
BIOS	Based on AMIBIOS [®] -1MByte Flash BIOS with congatec Embedded BIOS features
Power Management	ACPI 2.0 compliant

 **Note**

Some of the features mentioned in the above Feature Summary are optional. Check the article number of your module and compare it to the option information list on page 7 of this user's guide to determine what options are available on your particular module.

1.2 Supported Operating Systems

The conga-E852/855 supports the following operating systems.

- Microsoft® Windows® XP/2000
- Microsoft® Windows® XP Embedded
- Microsoft® Windows® CE 5.0
- Windriver VXWorks
- Linux
- QNX

1.3 Mechanical Dimensions

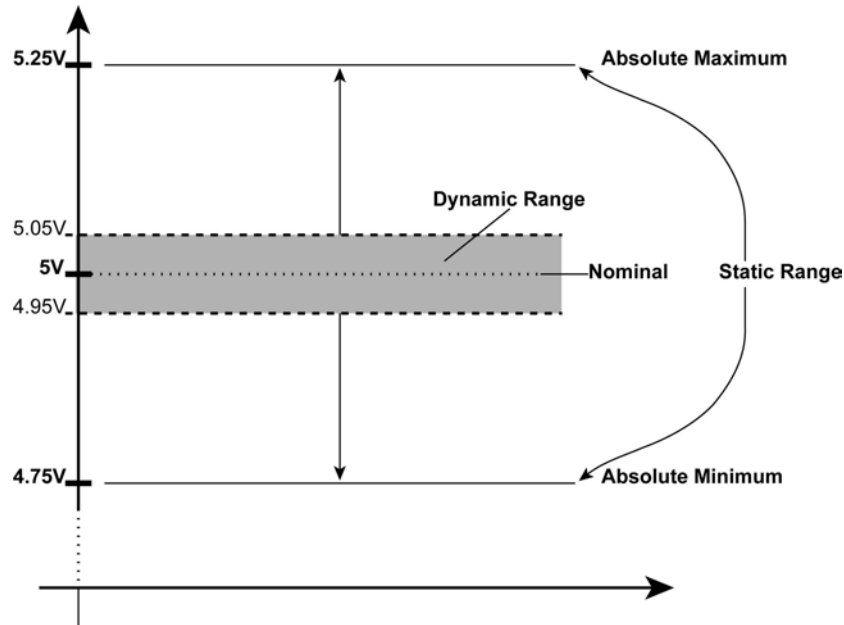
- 95.0 mm x 114.0 mm (3.75" x 4.5")
- Height approx. 12mm (0.4")

1.4 Electrical Characteristics

Characteristics			Min	Typ	Max	Units	Comment
5V	Voltage	+/-5%	4.75	5.00	5.25	Vdc	
	Ripple		-	-	100	mV _{pp}	0-20MHz
	Current	See section 1.5 'Power Consumption' for supply current information.					
5V_SB	Voltage	+/-5%	4.75	5.00	5.25	Vdc	
	Current			100	250	mA	

1.4.1 Supply Voltage Ripple

You must ensure that the dynamic range does not exceed the static range.



1.5 Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The ETX[®] module was mounted into a special baseboard. This baseboard has two Hirose connectors that connect to the corresponding X3 and X4 connectors on the module. The special baseboard does not have any power consuming components mounted on it. It provides one connector for a CRT monitor connection, a PS2 keyboard and mouse connection, and an IDE device connection. The baseboard is powered by a Direct Current (DC) power supply that is set to output 5 Volts and is connected directly to the special baseboard. Additionally, positive and negative sense lines are connected to the baseboard in order to measure the current consumption of the module. This current consumption value is displayed by the DC power supply's readout and this is the value that is recorded as the power consumption measurement. All recorded values are approximate.

All external peripheral devices, such as the hard drive, are externally powered so that they do not influence the power consumption value that is measured for the module. This ensures the value measured reflects the true power consumption of the module and only the module. A keyboard is used to configure the module and then it is disconnected before the measurement is recorded. If the keyboard remained connected, an additional current consumption of approximately 10 mA is noticed.

Each module was measured while running Windows XP Professional with SP2 (service pack 2) and the "Power Scheme" was set to "Portable/Laptop". This setting ensures that Pentium M processors reduce their output to 600MHz during desktop idle. Celeron M processors do not support this feature and therefore run at full speed even during

desktop idle. The screen resolution was set to 800x600 32bit High Color. Each conga-E852 variant was tested while using a swissbit® DDR1 PC2700 512MB memory module. Using different sizes of RAM will cause slight variances in the measured results. Power consumption values were recorded during the following stages:

Windows XP Professional SP2

- Desktop Idle (600MHz for Pentium M, Maximum frequency for Celeron M)
- 100% CPU workload (*see note below*)
- Windows Standby (*see note below*)



A software tool was used to stress the CPU to 100% workload.

ACPI OS Standby = S1 = POS = CPU is in sleep mode (internal clocks stopped, no snoops)

Processor Information

In the following power tables there is some additional information about the processors. Intel® offers processors that are considered to be low power consuming. These processors can be identified by their voltage status. Intel uses the following terms to describe these processors. If none of these terms are used then the processor is not considered to be low power consuming.

LV=Low voltage
ULV=Ultra low voltage

When applicable, the above mentioned terms will be added to the power tables to describe the processor. For example:

Celeron M 1.0GHz 512kB L2 cache
ULV Min=0.876 Max=0.956 90nm

In each processor datasheet Intel® describes the core voltage (measured in volts V) of the processor. They list either the typical or minimum and maximum core voltage depending on the processor. The following terms are used:

Typ=Typical core voltage
Min=Minimum core voltage
Max=Maximum core voltage

This information is also included in the power tables for each processor. For example:

Celeron M 1.0GHz 512kB L2 cache
ULV Min=0.876 Max=0.956 90nm

Intel® also describes the type of manufacturing process used for each processor. The following term is used:

nm=nanometer

The manufacturing process description is included in the power tables as well. See example below. For information about the manufacturing process visit Intel®'s website.

Celeron M 1.0GHz 512kB L2 cache
 ULV Min=0.876 Max=0.956 **90nm**

1.5.1 conga-E852 600MHz 512kB L2 cache Article No. 016029

With 512MB memory installed

conga-E852 Article No. 016029	Celeron M 600MHz 512kB L2 cache ULV Typ=1.004 90nm Layout Rev. E852LA0 /BIOS Rev. E852R001		
Memory Size	512MB		
Operating System	Windows XP Professional SP2		
Power State	Desktop Idle	100% workload	Standby
Power consumption (measured in Amperes/Watts)	1.3-1.4 A/6.5 7 W	1.9 A/9.5 W	0.9 A/4.5 W

1.5.2 conga-E855 Celeron M 1.0GHz 512kB L2 cache Article No. 012347

With 512MB memory installed

conga-E855 Article No. 012347	Celeron M 1.0GHz 512kB L2 cache ULV Min=0.876 Max=0.956 90nm Layout Rev. E852LA0 /BIOS Rev. E852R001		
Memory Size	512MB		
Operating System	Windows XP Professional SP2		
Power State	Desktop Idle	100% workload	Standby
Power consumption (measured in Amperes/Watts)	TBD	TBD	TBD

1.5.3 conga-E855 Pentium M 1.1GHz 1MB L2 cache Article No. 024714

With 512MB memory installed

conga-E855 Article No. 024714	Pentium M 1.1GHz 1MB L2 cache ULV Typ=1.004 130nm Layout Rev. E852LA0 /BIOS Rev. E852R001		
Memory Size	512MB		
Operating System	Windows XP Professional SP2		
Power State	Desktop Idle (600MHz)	100% workload	Standby
Power consumption (measured in Amperes/Watts)	TBD	TBD	TBD

1.5.4 conga-E855 Pentium M 1.4GHz 2MB L2 cache Article No. 034712

With 512MB memory installed

conga-E855 Article No. 034712	Pentium M 1.4GHz 2MB L2 cache LV Typ=1.116 90nm Layout Rev. E852LA0 /BIOS Rev. E852R001		
Memory Size	512MB		
Operating System	Windows XP Professional SP2		
Power State	Desktop Idle (600MHz)	100% workload	Standby
Power consumption (measured in Amperes/Watts)	TBD	TBD	TBD

1.5.5 conga-E855 Pentium M 1.6GHz 1MB L2 cache Article No. 024172

With 512MB memory installed

conga-E855 Article No. 024172	Pentium M 1.6GHz 1MB L2 cache Typ=1.484 130nm Layout Rev. E852LA0 /BIOS Rev. E852R001		
Memory Size	512MB		
Operating System	Windows XP Professional SP2		
Power State	Desktop Idle (600MHz)	100% workload	Standby
Power consumption (measured in Amperes/Watts)	TBD	TBD	TBD

 **Note**

All of the above recorded values are approximate.

1.6 Supply Voltage Battery Power

- 2.0V-3.6V DC
- Typical 3.0V

1.6.1 CMOS Battery Power Consumption

RTC @ 20°C	Voltage	Current
Integrated in the Intel® I/O Controller Hub 82801DB (ICH4)	3V DC	3.20 µA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec AG website at www.congatec.com.

1.7 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Note

The above operating temperatures must be strictly adhered to at all times. When using a heatspreader the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

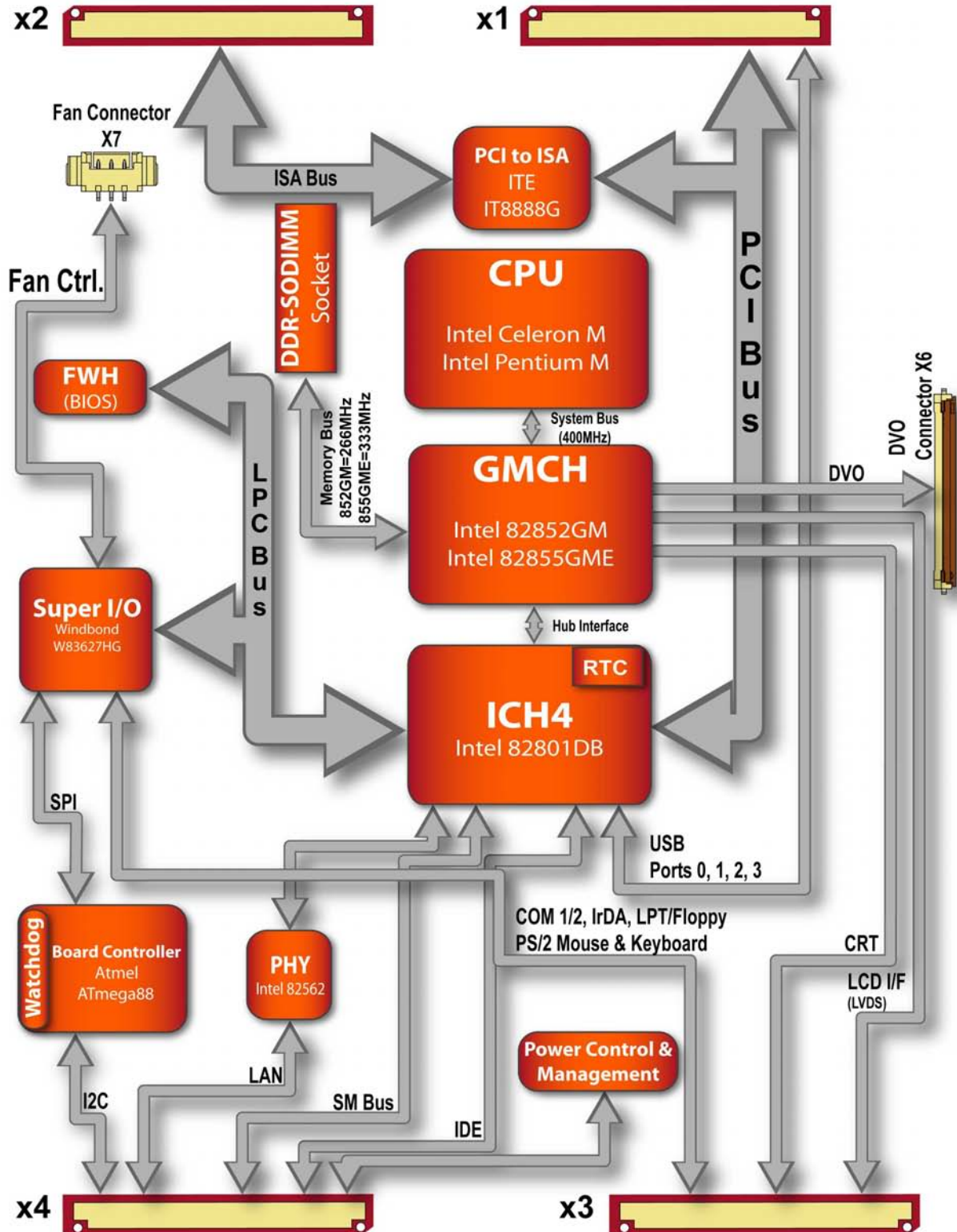
congatec AG strongly recommends that you use the appropriate congatec module heatspreader as a thermal interface between the module and your application specific cooling solution.

If for some reason it is not possible to use the appropriate congatec module heatspreader, then it is the responsibility of the operator to ensure that all components found on the module operate within the component manufacturer's specified temperature range.

For more information about operating a congatec module without heatspreader contact congatec technical support.

Humidity specifications are for non-condensing conditions.

2 Block Diagram



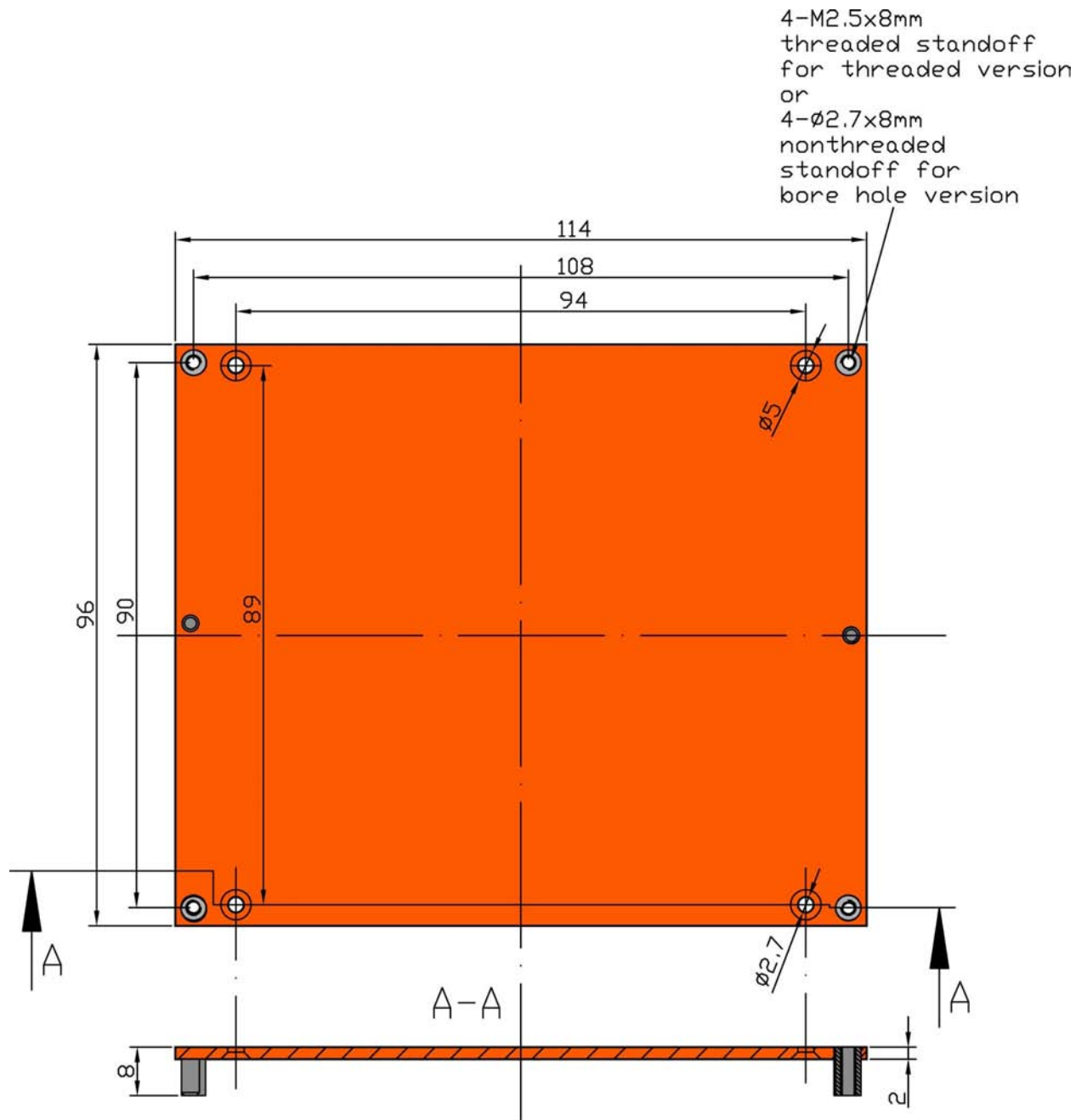
3 Heatspreader

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module. It is a 2mm thick aluminum plate. Due to the thickness of the plate all hardware components located beneath the heatspreader should not exceed a height of 6mm. If there are hardware components that do exceed a height of 6mm, then it is possible to implement clearance holes but the mechanical integrity of the heatspreader must be maintained and the components should not exceed a maximum height of 8mm. A heatspreader may also have an access hole so that the memory socket can be accessed when the heatspreader is mounted to the module, but again you must ensure that the mechanical integrity of the heatspreader plate is not compromised.

The heatspreader is thermally coupled to the CPU via a thermal gap filler and on some modules it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed to be used as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis therefore using the whole chassis as a heat dissipater.

3.1 Heatspreader Dimensions

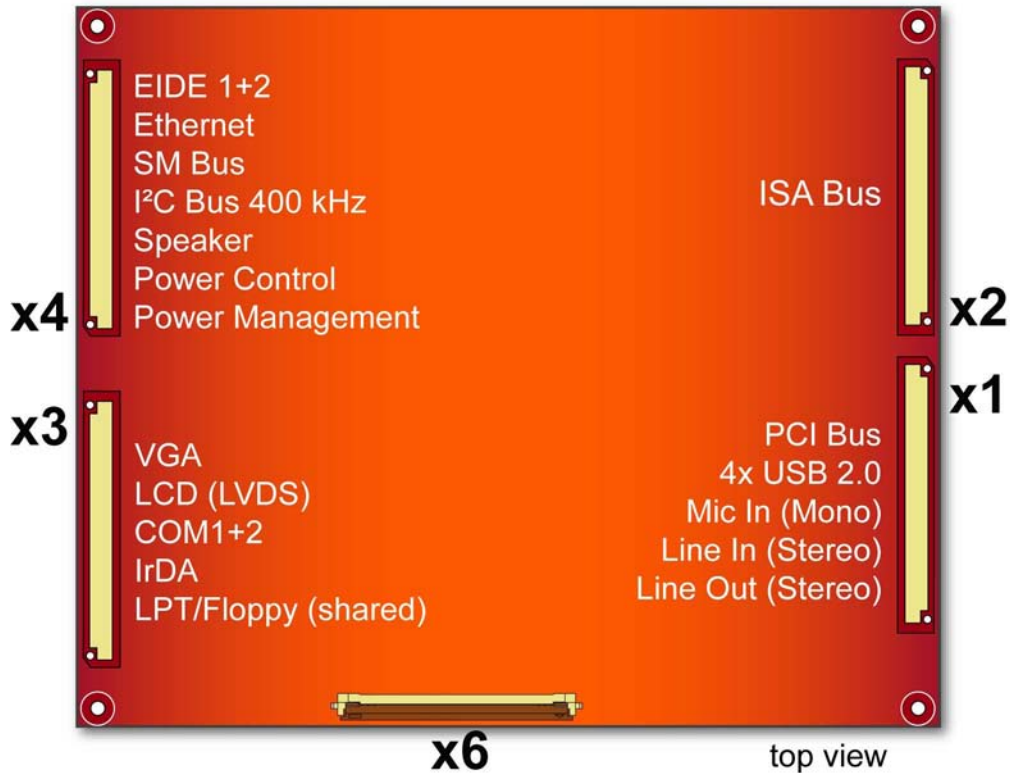


 **Note**

All measurements are in millimeters. Torque specification for heatspreader screws is 0.5 Nm.

4 Connector Subsystems

X connector Subsystems (top view)



In this view the connectors are seen “through” the module.

4.1 Connector X1

The following subsystems can be found on connector X1.

4.1.1 PCI Bus

The implementation of the PCI bus complies with PCI specification Rev. 2.1 and ETX[®] specification Rev. 2.7

4.1.2 USB 2.0

The conga-E852/855 offers three UHCI USB host controllers and one EHCI USB host controller via the Intel[®] 82801DB (ICH4). These controllers comply with USB standard 1.1 and 2.0. Four USB ports are located on the X1 connector. For more information about how the USB host controllers are routed see section 6.7.

4.1.3 Audio

The conga-E852/855 is equipped with a Realtek ALC655 PCI audio controller. It is AC'97 2.2 specification compliant and legacy audio SB16™ compatible.

**Note**

The USB and Audio controllers are PCI bus devices. The BIOS allocates the necessary system resources when configuring the PCI devices.

4.1.4 Onboard Generated Supply Voltage

Pins 12, 16 and 24 on the X1 connector provide the ability to connect external devices to the modules onboard generated supply voltage ($3.3V \pm 5\%$). 3.3V external devices can be connected to these pins but must not exceed a maximum external load of 500mA. For more information about this feature contact congatec AG technical support.

**Note**

Do not connect pins 12, 16 and 24 to a 3.3V external power supply.

4.2 Connector X2 (ISA Bus)

4.2.1 ISA Bus

The ISA bus on the conga-E852/855 is implemented through the use of an ITE IT8888G PCI to ISA bridge device.

4.3 Connector X3

The following subsystems can be found on connector X3. The implementation of all the subsystems comply with ETX[®] specification 2.7. The different subsystems require I/O and IRQ resources. The necessary resources are allocated by the BIOS during the POST routine and are configured to be compatible to common PC/AT settings. You can use the BIOS setup to configure some of the parameters that relate to the specific subsystems. Check the BIOS Setup Description section for more information about how to configure a particular subsystem.

4.3.1 Graphics

The conga-E852/855 graphics are driven by an Intel[®] Extreme Graphics[®] engine, which is incorporated into the Intel[®] 82852GM/82855GME chipset on the conga-E852/855.

4.3.2 LCD

The Intel[®] 82852GM/82855GME chipset, found on the conga-E852/855, offers an integrated dual channel LVDS interface supported on Display Pipe B only.

4.3.3 Serial Ports (1 and 2)

The conga-E852/855 offers two serial interfaces (TTL) that are provided by the I/O controller, which is a Winbond W83627HG super I/O located on the conga-E852/855.

4.3.4 Serial Infrared Interface

Serial port 2 can be configured as a serial infrared interface. The Infrared (IrDA) function provides point-to-point (or multi-point to multi-point) wireless communication, which can operate under various transmission protocols including IrDA SIR. This feature is also implemented by the onboard Winbond W83627HG super I/O.

4.3.5 Parallel Port/Floppy Interface

The parallel port/floppy interface can be configured as either a conventional LPT parallel port or a floppy-disk drive port. This is software implemented and can be configured in the BIOS setup program. See section 9.4.6 of this document for information about configuring the parallel port/floppy interface.

4.3.6 Keyboard/Mouse

The implementation of these subsystems comply with ETX[®] specification 2.7.

4.4 Connector X4

The following subsystems can be found on connector X4. The implementation of all the subsystems comply with ETX[®] specification 2.7. The different subsystems require I/O and IRQ resources. The necessary resources are allocated by the BIOS during the POST routine and are configured to be compatible to common PC/AT settings. You can use the BIOS setup to configure some of the parameters that relate to the specific subsystems. Check the BIOS Setup Description section for more information about how to configure a particular subsystem.

4.4.1 IDE

The IDE host adapter is capable of UDMA-100 operation.

4.4.2 Ethernet

Ethernet interface is provided by an Intel[®] 82562 integrated Fast Ethernet NIC controller. The controller is IEEE 802.3u, 10/100Base-Tx fast Ethernet compatible. The interface provides single-ended differential signals that have to be routed through an Ethernet transformer.

4.4.3 I²C Bus 400kHz

The I²C bus is implemented through the use of ATMEL ATmega88 microcontroller. It provides a Fast Mode (400kHz max.) multi-master I²C Bus that has maximum I²C bandwidth.

4.4.4 Power Control

PWGIN

PWGIN (pin 4 on the X4 connector) can be connected to an external power good circuit or it may also be utilized as a manual reset input. In order to use PWGIN as a manual reset the pin must be grounded through the use of a momentary-contact pushbutton switch. When external circuitry asserts this signal, it's necessary that an open-drain driver drives this signal causing it to be held low for a minimum of 15ms to initiate a reset. Using this input is optional. Through the use of an internal monitor on the +5V input voltage and/or the internal power supplies the conga-E852/855 module is capable of generating its own power-on reset.

The conga-E852/855 provides support for controlling ATX-style power supplies. In order to do this the power supply must provide a constant source of 5V power. When not using an ATX power supply then the conga-E852/855's pins PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

PS_ON#

The PS_ON (pin 5 on the X4 connector) signal is an active-low output that turns on the main outputs of an ATX-style power supply. This open-collector signal can be pulled up to the 5V_SB supply voltage through the use of a 1K resistor. Usually there is a pull-up resistor internally implemented in the power supply itself yet it is also good practice to implement a footprint for the pull-up resistor in the baseboard circuitry.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin 7 on the X4 connector) is used to connect to a momentary-contact, active-low pushbutton input while the other terminal on the pushbutton must be connected to ground. This signal is ETX[®] internally pulled up to 5V_SB using a 4k7 resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

5 volt input power is the sole operational power source for the conga-E852/855. The remaining necessary voltages are internally generated on the module using onboard power supplies. A baseboard designer should be aware of the following important information when designing a power supply for a conga-E852/855 application:

- As mentioned earlier in section 4.1.4 the conga-E852/855 is capable of generating an onboard 3.3V supply with an output current that is limited to 500mA. If an external device requires more than this 500mA limit then it's necessary to design a 3.3V supply into the baseboard.



Caution

It is not possible to connect an external 3.3V supply to the onboard generate 3.3V supply pins on the conga-E852/855 module. This will cause the current cross-flow and

may result in either a system malfunction and/or damage to the external power supply and the module.

- Sometimes when designing baseboards, baseboard designers choose to fuse power to some external devices such as keyboards or USB devices by using solid-state or polyswitch overcurrent protection devices. This results in the protective devices typically only opening after they pass several times their rated current for long periods of time. When the application power supply is incapable of generating the necessary current needed to open these protective devices it's possible that the application crashes as a result of an external fault and therefore will reduce the applications reliability as well as make a fault diagnosis of the application difficult.
- It has also been noticed that on some occasions problems occur when using a 5V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document "ATX12V Power Supply Design Guide V2.2".

4.4.5 Power Management

APM 1.2 compliant. ACPI 2.0.

5 Additional Features

5.1 Watchdog

The conga-E852/855 is equipped with a multi stage watchdog. This solution can be triggered by software and external OEM hardware (input pin is pin 48 on the X2 connector called WDTRG#). For more information about the Watchdog feature see the BIOS setup description section 9.4.13 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

5.2 Onboard Microcontroller

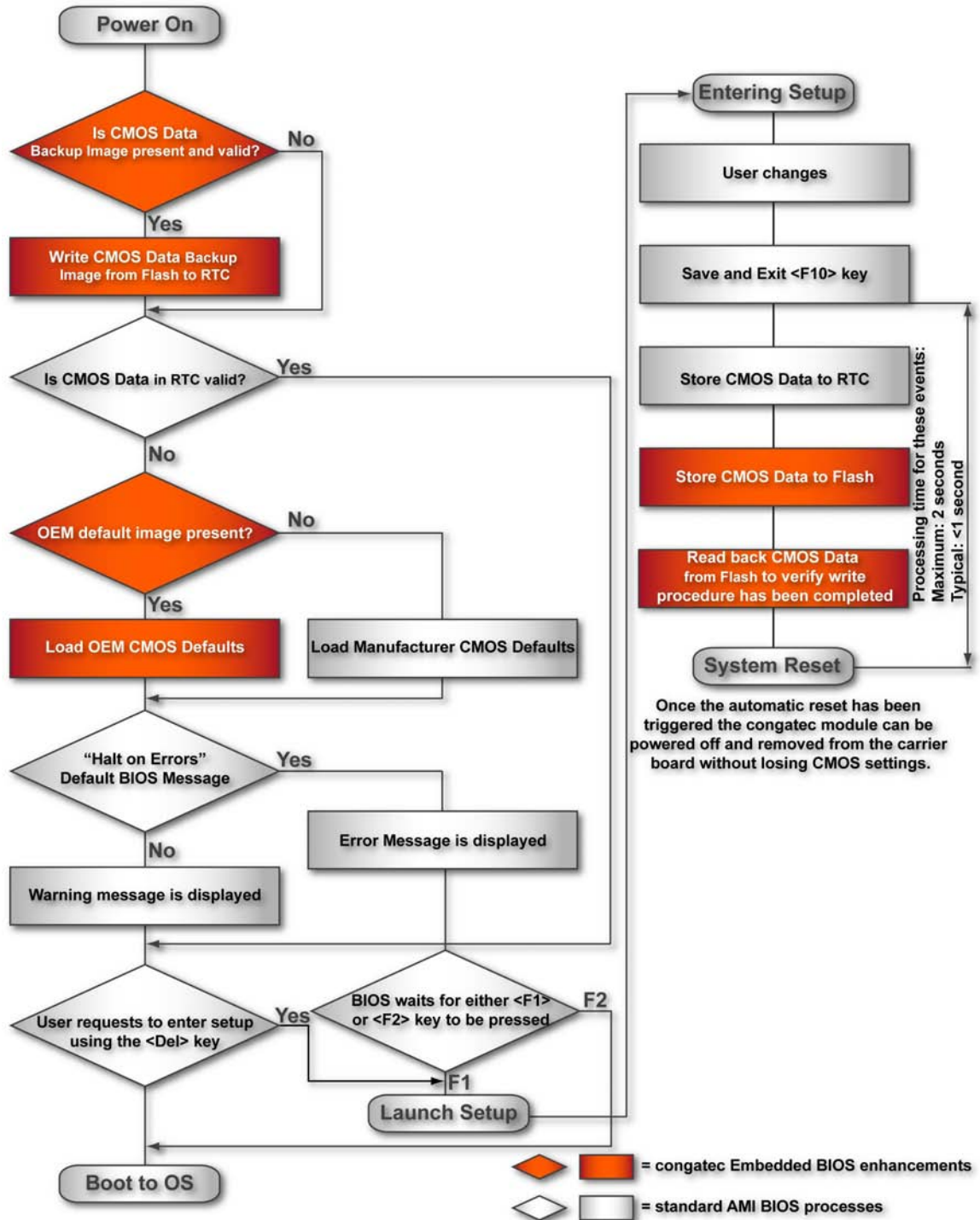
The conga-E852/855 is equipped with an ATMEL Atmega88 microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in standby mode.

5.3 Embedded BIOS

The conga-E852/855 is equipped with congatec Embedded BIOS and has the following features:

- ACPI Power Management
- Supports Customer Specific CMOS Defaults
- Multistage Watchdog
- User Data Storage
- Manufacturing Data and Board Information
- OEM Splash Screen
- Flat Panel Auto Detection
- BIOS Setup Data Backup (see section 5.3.1)
- Fast Mode I²C Bus
- Real Headless Operation
- Console Redirection and BIOS Update (flashing BIOS) via Serial Port

5.3.1 Simplified Overview of BIOS Setup Data Backup



The above diagram provides an overview of how the BIOS Setup Data is backed up on congatec modules. OEM default values mentioned above refer to customer specific CMOS settings created using the congatec System Utility tool.

Once the BIOS Setup Program has been entered and the settings have been changed, the user saves the settings and exits the BIOS Setup Program using the F10 key feature. After the F10 function has been evoked, the CMOS Data is stored in a dedicated non-volatile CMOS Data Backup area located in the BIOS Flash ROM chip as well as RTC. The CMOS Data is written to and read back from the CMOS Data Backup area and verified. Once verified the F10 Save and Exit function continues to perform some minor processing tasks and finally reaches an automatic reset point, which instructs the module to reboot. After the Automatic Reset has been triggered the congatec module can be powered off and if need be removed from the baseboard without losing the new CMOS settings.

5.4 DVO

The conga-E852/855 provides one DVO port (DVO C), which is implemented by the Intel 82852GM/82855GME. This interface is available via a connector (X6) located on the bottom side of conga-E852/855. The DVO interface is compliant with DVI specification 1.0. This port can be driven on Pipe A or Pipe B. For information about the pinout of the X6 connector see section 7.8.

6 conga Tech Notes

The conga-E852/855 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the System Resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

6.1 Comparison of I/O APIC to 8259 PIC Interrupt mode

I/O APIC (Advanced Programmable Interrupt controller) mode deals with interrupts differently than the 8259 PIC.

The method of interrupt transmission used by APIC mode is implemented by transmitting interrupts through the system bus and they are handled without the requirement of the processor to perform an interrupt acknowledge cycle.

Another difference between I/O APIC and 8259 PIC is the way the interrupt numbers are prioritized. Unlike the 8259 PIC, the I/O APIC interrupt priority is independent of the actual interrupt number.

A major advantage of the I/O APIC found in the chipset of the conga-E852/855 is that it's able to provide more interrupts, a total of 24 to be exact. It must be mentioned that the APIC is not supported by all operating systems. In order to utilize the APIC mode it must be enabled in the BIOS setup program before the installation of the OS and it only functions in ACPI mode. You can find more information about APIC in the IA-32 Intel Architecture Software Developer's Manual, Volume 3 in chapter 8.

Note

You must ensure that your operating system supports APIC mode in order to use it.

6.2 Native vs. compatible IDE mode

6.2.1 Compatible Mode

When operating in compatible mode, the PATA controller needs two legacy IRQs (14 and 15) and is unable to share these IRQs with other devices. This is a result of the fact that the PATA controller emulates a legacy IDE controller that is a non-standard extension of the ISA based IDE controller.

6.2.2 Native Mode

Native mode allows the PATA controller to operate as a true PCI device and therefore does not need dedicated legacy resources, which means it can be configured anywhere within the system. When the PATA controller runs in native mode it only requires one PCI interrupt for both channels and also has the ability to share this interrupt with other devices in the system.

Running in native mode frees up interrupt resources (IRQs 14 and 15) and decreases the chance that there may be a shortage of interrupts when installing devices.

 **Note**

If your operating system supports native mode then congatec AG recommends you enable it.

6.3 Thermal Monitor and Catastrophic Thermal Protection

Pentium/Celeron M processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature, that the Intel Thermal Monitor uses to activate the TCC, cannot be configured by the user nor is it software visible.

The Thermal Monitor can control the processor temperature through the use of two different methods defined as TM1 and TM2. TM1 method consists of the modulation (starting and stopping) of the processor clocks at a 50% duty cycle. The TM2 method initiates an Enhanced Intel Speedstep transition to the lowest performance state once the processor silicon reaches the maximum operating temperature.

 **Note**

The maximum operating temperature for Pentium/Celeron M processors is 100°C. TM2 mode should be used for Intel Pentium M processors and is only supported by Intel Pentium M processors, it is not supported by Intel Celeron M processors.

Two modes are supported by the Thermal Monitor to activate the TCC. They are called Automatic and On-Demand. In order for the processor to operate within specification, the Intel Thermal Monitor Automatic Mode must be enabled through a setup node in the BIOS. No additional hardware, software, or handling routines are necessary when using Automatic Mode.

 **Note**

To ensure that the TCC is active for only short periods of time thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel Pentium/Celeron M processors datasheet can provide you with more information about this subject.

THERMTRIP# signal is used by Intel's Pentium/Celeron M processors for catastrophic thermal protection. If the processor's silicon reaches a temperature of approximately 125°C then the processor signal THERMTRIP# will go active and the system will automatically shut down to prevent any damage to the processor as a result of overheating. The THERMTRIP# signal activation is completely independent from processor activity and therefore does not produce any bus cycles.

 **Note**

In order for THERMTRIP# to be able to automatically switch off the system it is necessary to use an ATX style power supply.

6.4 Processor Performance Control

Pentium M processors run at different voltage/frequency states (performance states), which is referred to as Enhanced Intel® SpeedStep® technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states in order to efficiently operate the processor when it's not being fully utilized. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime.

The Windows family of operating systems links its processor performance control policy to the power scheme setting found in the control panel option applet.



Note

If the "Home/Office" or "Always On" power scheme is selected when using Windows operating systems then the processor will always run at the highest performance state. For more information about this subject see chapter 8 of the ACPI Specification Revision 2.0c, which can be found at www.acpi.info. Also visit Microsoft's website and search for the document called "Windows Native Processor Performance Control".

The congatec BIOS allows you to limit the maximum processor frequency. This can be useful if the maximum performance is not required or if the maximum processor performance state dissipates too much power and heat.

In the 'CPU Configuration' submenu of the 'BIOS Setup Program' you'll find the node for 'Max. Frequency' limitation. For each Pentium M processor the BIOS lists the supported frequencies. If a lower frequency than the maximum one is selected, the processor will never run at frequencies above this setting.

Celeron M processors do not support Enhanced Intel® SpeedStep® technology. They always run at a fixed frequency. In order to limit the performance and power consumption of Celeron M processors, the congatec BIOS offers 'On-Demand Clock Modulation' support in the 'CPU Configuration' sub menu of the 'BIOS Setup Program'. When 'On-Demand Clock Modulation' is enabled, the processor clock is throttled using the duty cycle determined in setup. Keep in mind that the 'On-Demand' clock modulation duty cycle indicates that the clock on to clock off interval ratio. This means that when set to 75% the clock is running 75% of the overall time and this leads to a performance decrease of approximately 25%.

On the conga-E852/855 variant that is equipped with a Celeron M 600MHz 512 L2 cache CPU (article number 016029), the power consumption decreases approximately 0.5W when set to 75% duty cycle and 1.0W when set to 50% duty cycle.

6.5 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

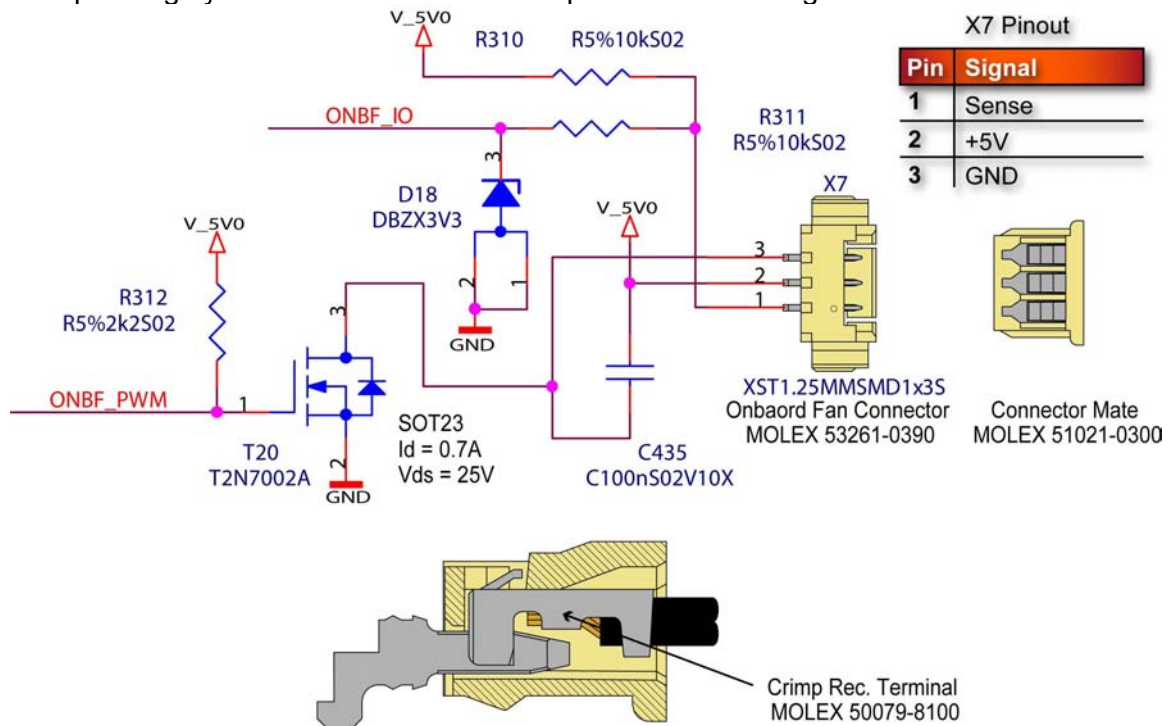
The conga-E852/855 ACPI thermal solution offers three different cooling policies.

- Passive Cooling

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- Active Cooling

The conga-E852/855 is equipped with an onboard fan connector that is described in the diagram below. During an active cooling policy the operating system is turning the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the "active cooling trip point" setup node in the BIOS setup description section 9.4.1 to determine the temperature threshold that the operating system will use to start or stop the active cooling device.



- Critical Trip Point

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the “critical trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

 **Notes**

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled according to the formula below.

$$\Delta P[\%] = TC1(T_n - T_{n-1}) + TC2(T_n - T_t)$$

- ΔP is the performance delta
- T_t is the target temperature = critical trip point.
- The two coefficients TC1 and TC2 and the sampling period TSP are hardware dependent constants and are set to fixed values for the conga-E852/855:
- TC1= 1
- TC2= 5
- TSP= 5 seconds

See section 12 of the ACPI Specification 2.0 C for information about passive cooling.

6.6 ACPI Suspend Modes and Resume Events

conga-E852/855 only supports the S1 (POS= Power On Suspend) state. S3 (STR= Save to Ram) is not supported. S4 (Save to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems (S4_OS= Hibernate):

- Win2K
- WinXP

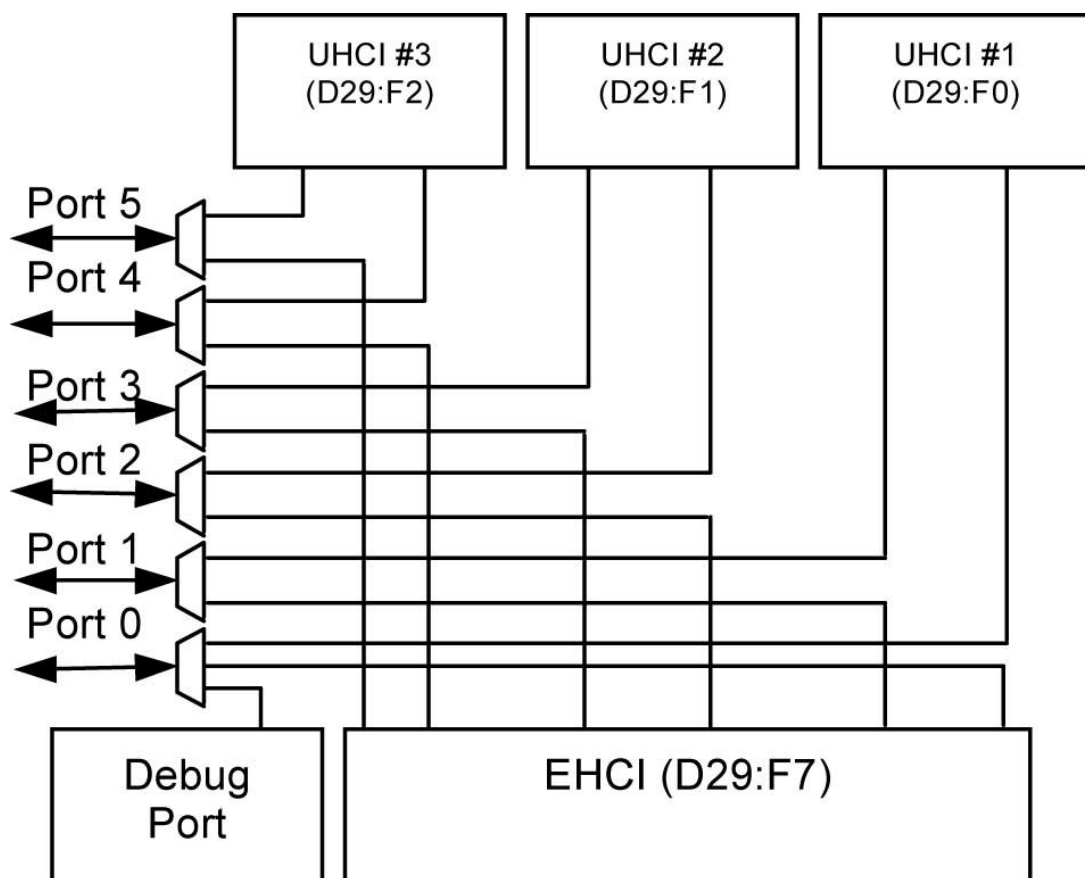
The following events resume the system from S1:

- Power button
- PS2 keyboard and mouse (IRQs 1 and 12)
- USB Wake Events
- PCI Bus signal PME#

6.7 USB 2.0 EHCI Host Controller Support

The 6 USB ports are shared between an EHCI host controller and the 3 UHCI host controllers. Within the EHC functionality there is a port-routing logic that executes the mixing between the two different types of host controllers (EHCI and UHCI). This means that when a USB device is connected the routing logic determines who owns the port. If the device is not USB 2.0 compliant, or if the software drivers for EHCI support are not installed, then the UHCI controller owns the ports.

Routing Diagram:



7 Signal Descriptions and Pinout Tables

The following section describes the signals found on the four X connectors located on the bottom of the module.

This table describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if an ETX[®] internal pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented.

The “#” symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When “#” is not present, the signal is asserted when at a high voltage level.

Table 2 Signal Tables Terminology Descriptions

Term	Description
PU	ETX [®] Internally implemented Pull up resistor
PD	ETX [®] Internally implemented Pull down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
P	Power Input/Output
DDC	Display Data Channel
LVDS	Low Voltage Differential Signal-350mV nominal; 450mV maximum differential signal

7.1 X1 Connector Signal Descriptions

Table 3 Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
VCC	Power Supply +5VDC ±5%	P		External supply
GND	Power Ground	P		External supply
3V	Power Supply +3.3VDC	P		See section 4.1.4
N.C.	Not Connected or internally connected	N.A.		Do not connect on baseboard
SERRIRQ	Serial Interrupt request	I 3.3V	PU 8k2 3.3V	Used in conjunction with LPC bus

Table 4 PCI Signal Descriptions

Signal	Description of PCI Bus Signals	I/O	PU/PD	Comment
PCICLK1..4.	Clock output	O 3.3V		Check length restriction in design guide
REQ0..3#	Bus request	I 3.3V	PU 8k2 3.3V	5V tolerant
GNT0..3#	Bus grant	O 3.3V		
AD0..31	Address/Data bus lines	I/O 3.3V		5V tolerant
CBE0..3#	Bus command/byte enables	I/O 3.3V		5V tolerant
PAR	Bus parity	I/O 3.3V		5V tolerant
SERR#	Bus system error	I/O 3.3V	PU 8k2 3.3V	5V tolerant
GPERR#	Bus grant parity error	I/O 3.3V	PU 8k2 3.3V	5V tolerant
PME#	Bus power management event	I/O 3.3V	PU 8k2 3.3V	5V tolerant
LOCK#	Bus lock	I/O 3.3V)	PU 8k2 3.3V	5V tolerant
DEVSEL#	Bus device select	I/O 3.3V	PU 8k2 3.3V	5V tolerant
TRDY#	Bus target ready	I/O 3.3V	PU 8k2 3.3V	5V tolerant
IRDY#	Bus initiator ready	I/O 3.3V	PU 8k2 3.3V	5V tolerant
STOP#	Bus stop	I/O 3.3V	PU 8k2 3.3V	5V tolerant
FRAME#	Bus frame	I/O 3.3V	PU 8k2 3.3V	5V tolerant
PCIRST#	Bus reset	O 3.3V		
INTA#	Bus interrupt A	I 3.3V	PU 8k2 3.3V	5V tolerant
INTB#	Bus interrupt B	I 3.3V	PU 8k2 3.3V	5V tolerant
INTC#	Bus interrupt C	I 3.3V	PU 8k2 3.3V	5V tolerant
INTD#	Bus interrupt D	I 3.3V	PU 8k2 3.3V	5V tolerant

Table 5 USB Signal Descriptions

Signal	Description of USB Signals	I/O	PU/PD	Comment
USB0	USB Port 0, data + or D+	I/O 3.3V		Differential Pair, USB 2.0 compliant and backwards compatible to USB 1.1
USB0#	USB Port 0, data - or D-	I/O 3.3V		
USB1	USB Port 1, data + or D+	I/O 3.3V		Differential Pair, USB 2.0 compliant and backwards compatible to USB 1.1
USB1#	USB Port 1, data - or D-	I/O 3.3V		
USB2	USB Port 2, data + or D+	I/O 3.3V		Differential Pair, USB 2.0 compliant and backwards compatible to USB 1.1
USB2#	USB Port 2, data - or D-	I/O 3.3V		
USB3	USB Port 3, data + or D+	I/O 3.3V		Differential Pair, USB 2.0 compliant and backwards compatible to USB 1.1
USB3#	USB Port 3, data - or D-	I/O 3.3V		

Table 6 Audio Signal Descriptions

Signal	Description of Audio Signals	I/O	PU/PD	Comment
SNDL	Line-Level stereo output left	O		Analog output (1 Vrms)
SNDR	Line-Level stereo output right	O		Analog output (1 Vrms)
AUXAL	Auxiliary input A left	I	22k PD	Analog input (1 Vrms)
AUXAR	Auxiliary input A right	I	22k PD	Analog input (1 Vrms)
MIC	Microphone input	I	2k2 PU AudioVref	Analog input (1 Vrms)
ASGND	Analog ground of sound controller	P		
ASVCC	Analog supply of sound controller	P		Internally connected to +3.3 audio voltage for reference, max. 10mA

7.2 Connector X1 Pinout

Table 7 X1 Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	VCC	52	VCC
3	PCICLK3	4	PCICLK4	53	PAR	54	SERR#
5	GND	6	GND	55	GPERR#	56	Reserved
7	PCICLK1	8	PCICLK2	57	PME#	58	USB2#
9	REQ3#	10	GNT3#	59	LOCK#	60	DEVSEL#
11	GNT2#	12	3V	61	TRDY#	62	USB3#
13	REQ2#	14	GNT1#	63	IRDY#	64	STOP#
15	REQ1#	16	3V	65	FRAME#	66	USB2
17	GNT0#	18	RESERVED	67	GND	68	GND
19	VCC	20	VCC	69	AD16	70	CBE2#
21	SERIRQ	22	REQ0#	71	AD17	72	USB3
23	AD0	24	3V	73	AD19	74	AD18
25	AD1	26	AD2	75	AD20	76	USB0#
27	AD4	28	AD3	77	AD22	78	AD21
29	AD6	30	AD5	79	AD23	80	USB1#
31	CBE0#	32	AD7	81	AD24	82	CBE3#
33	AD8	34	AD9	83	VCC	84	VCC
35	GND	36	GND	85	AD25	86	AD26
37	AD10	38	AUXAL	87	AD28	88	USB0
39	AD11	40	MIC	89	AD27	90	AD29
41	AD12	42	AUXAR	91	AD30	92	USB1
43	AD13	44	ASVCC	93	PCIRST#	94	AD31
45	AD14	46	SNDL	95	INTC#	96	INTD#
47	AD15	48	ASGND	97	INTA#	98	INTB#
49	CBE1#	50	SNDR	99	GND	100	GND

7.3 X2 Connector Signal Descriptions

Table 8 Signal Descriptions

Signal	Description	I/O	Comment
VCC	Power Supply +5VDC, ±5%	I	External supply
GND	Power Ground	I	External supply
N.C.	Not connected	N.A.	Do not connect

Table 9 ISA Bus Signal Descriptions

Signal	Description of ISA Bus Signals	I/O	PU/PD	Comment
SD0..15	ISA Data bus	I/O 5V	PU 10k 5V	
SA0..19, LA17..20	ISA Address bus	O 5V		
SBHE#	ISA Byte High Enable	O 5V	PU 10k 5V	
BALE	ISA Address Latch Enable	O 5V	PD 10k	BALE is a boot strap signal (see note below)
AEN	ISA Address Enable	O 5V	PD 10k	AEN is a boot strap signal (see note below)
MEMR#	ISA memory read	O 5V	PU 10k 5V	
SMEMR#	ISA memory read in lowest 1MB address range	O 5V	PU 10k 5V	
MEMW#	ISA memory write	O 5V	PU 10k 5V	
SMEMW#	ISA memory write in lowest 1MB address range	O 5V	PU 10k 5V	
IOR#	ISA IO read	O 5V	PU 10k 5V	
IOW#	ISA IO write	O 5V	PU 10k 5V	
IOCHK#	ISA IO check	I 5V	PU 10k 5V	
IOCHRDY	ISA IO channel ready	I 5V	PU 1k 5V	
M16#	ISA 16Bit memory device	I 5V	PU 330R 5V	
IO16#	ISA 16Bit IO device	I 5V	PU 330R 5V	
REFSH#	ISA memory refresh cycle pending	O 5V	PU 1k 5V	
NOWS#	ISA No wait states	I 5V	PU 330R 5V	
MASTER#	ISA Master	I 5V	PU 330R 5V	
SYSCLK	ISA System clock (8 MHz)	O 5V		
OSC	ISA Oscillator (14,31818 MHz)	O 5V		
RSTDRV	ISA Reset signal	O 5V		
DREQ [0,1,2,3,5,6,7]	ISA DMA request	I 5V	PD 10k	
DACK# [0,1,2,3,5,6,7]	ISA DMA acknowledge	O 5V		
TC	ISA DMA end	O 5V	PD 10k	TC is a boot strap signal (see note below)
IRQ [3..7, 9..15]	ISA Interrupt request	I/O 5V		

 **Note**

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.9 of this user's guide.

7.4 X2 Connector Pinout

Table 10 Connector X2 Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	VCC	52	VCC
3	SD14	4	SD15	53	SA6	54	IRQ5
5	SD13	6	MASTER#	55	SA7	56	IRQ6
7	SD12	8	DREQ7	57	SA8	58	IRQ7
9	SD11	10	DACK7#	59	SA9	60	SYSCLK
11	SD10	12	DREQ6	61	SA10	62	REFSH#
13	SD9	14	DACK6#	63	SA11	64	DREQ1
15	SD8	16	DREQ5	65	SA12	66	DACK1#
17	MEMW#	18	DACK5#	67	GND	68	GND
19	MEMR#	20	DREQ0	69	SA13	70	DREQ3
21	LA17	22	DACK0#	71	SA14	72	DACK3#
23	LA18	24	IRQ14	73	SA15	74	IOR#
25	LA19	26	IRQ15	75	SA16	76	IOW#
27	LA20	28	IRQ12	77	SA18	78	SA17
29	LA21	30	IRQ11	79	SA19	80	SMEMR#
31	LA22	32	IRQ10	81	IOCHRDY	82	AEN
33	LA23	34	IO16#	83	VCC	84	VCC
35	GND	36	GND	85	SD0	86	SMEMW#
37	SBHE#	38	M16#	87	SD2	88	SD1
39	SA0	40	OSC	89	SD3	90	NOWS#
41	SA1	42	BALE	91	DREQ2	92	SD4
43	SA2	44	TC	93	SD5	94	IRQ9 (**)
45	SA3	46	DACK2#	95	SD6	96	SD7
47	SA4	48	IRQ3	97	IOCHK#	98	RSTDRV
49	SA5	50	IRQ4	99	GND	100	GND

 **Note**

(**) When not using APIC mode, the ACPI SCI (System Control Interrupt) is routed to IRQ9 and therefore IRQ9 cannot be allocated to ISA bus devices. If using the APIC mode, the SCI can also be routed to IRQ 20 by enabling the "APIC ACPI SCI IRQ" BIOS setting (see section 9.4.5 of the BIOS Setup Description). The enabling of this setting allows IRQ9 to be allocated to ISA bus devices.

7.5 X3 Connector Signal Descriptions

Table 11 Signal Descriptions

Signal	Description	I/O	PU/PD	Comment
VCC	Power Supply +5VDC, $\pm 5\%$	P		External supply
GND	Power Ground	P		External supply
N.C.	Not connected	N.A.		Do not connect
LTGIO0	General Purpose I O	N.C.		Not supported

Table 12 CRT Signal Descriptions

Signal	Description of CRT signals	I/O	PU/PD	Comment
HSY	Horizontal Synchronization Pulse	O 5V		
VSY	Vertical Synchronization Pulse	O 5V		
R	Red channel RGB Analog Video Output	O		Analog output
G	Green channel RGB Analog Video Output	O		Analog output
B	Blue channel RGB Analog Video Output	O		Analog output
DDCK	Display Data Channel Clock	I/O 5V	PU 2k2 5V	
DDDA	Display Data Channel Data	I/O 5V	PU 2k2 5V	

Table 13 COM Signal Descriptions

Signal	Description of COM signals	I/O	PU/PD	Comment
DTR1#	Data terminal ready for COM1	O 5V	PU 4k7 5V	DTR1# is a boot strap signal (see note below)
DTR2#	Data terminal ready for COM2	O 5V	PD 100k	PD to keep signal from floating when not used
RI1#, RI2#	Ring indicator for COM1/COM2	I 5V	PD 100k	PD to keep signal from floating when not used
TXD1	Data transmit for COM1	O 5V	PU 4k7 5V	TXD1 is a boot strap signal (see note below)
TXD2	Data transmit for COM2	O 5V	PU 4k7 5V	TXD2 is a boot strap signal (see note below)
RXD1, RXD2	Data receive for COM1/COM2	I 5V		
CTS1#, CTS2#	Clear to send for COM1/COM2	I 5V	PD 100k	PD to keep signal from floating when not used
RTS1#, RTS2#	Request to send for COM1/COM2	O 5V	PD 100k	RTS1# is a boot strap signal (see note below) PD to keep signal from floating when not used
DCD1#, DCD2#	Data carrier detect for COM1/COM2	I 5V	PD 100k	PD to keep signal from floating when not used
DSR1#, DSR2#	Data set ready for COM1/COM2	I 5V	PD 100k	PD to keep signal from floating when not used

 **Note**

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.9 of this user's guide.

Table 14 Keyboard and Infrared Signal Descriptions

Signal	Description of keyboard and infrared signals	I/O	PU/PD	Comment
KBDAT	Keyboard Data	I/O 5V	PU 8k2 5V	
KBCLK	Keyboard Clock	O 5V	PU 8k2 5V	
MSDAT	Mouse Data	I/O 5V	PU 8k2 5V	
MSCLK	Mouse Clock	O 5V	PU 8k2 5V	
IRTX	Infrared Transmit	O 5V		Schmitt-trigger input
IRRX	Infrared Receive	I 5V		

Table 15 LVDS Flat Panel Signals

Signal	Description of LVDS Flat Panel signals	I/O	PU/PD	Comment
BIASON	Controls display contrast voltage ON	N.C.		Not supported
DIGON	Controls display Power ON	O 5V	PD 10k	
BLON#	Controls display Backlight ON	O 5V		
LCDD00..19	LVDS channel data 0..19	O LVDS		
DETECT#	Panel hot-plug detection	N.C.		Not supported
FPDDC_CLK	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k2 3.3V	
FPDDC_DAT	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	

Table 16 LVDS Interface Pinout

LVDS Interface Pinout			
Pin	Signal	Pin	Signal
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSY	8	DDCK
9	DETECT# (*)	10	DDDA
11	LCDDO16	12	LCDDO18
13	LCDDO17	14	LCDDO19
15	GND	16	GND
17	LCDDO13	18	LCDDO15
19	LCDDO12	20	LCDDO14
21	GND	22	GND
23	LCDDO8	24	LCDDO11
25	LCDDO9	26	LCDDO10
27	GND	28	GND
29	LCDDO4	30	LCDDO7
31	LCDDO5	32	LCDDO6
33	GND	34	GND
35	LCDDO1	36	LCDDO3
37	LCDDO0	38	LCDDO2
39	VCC	40	VCC
41	FPDDC DAT	42	LTGIO0 (*)
43	FPDDC CLK	44	BLON#
45	BIASON (*)	46	DIGON
47	COMP (*)	48	Y (*)
49	SYNC (*)	50	C (*)

 **Note**

The signals marked with an asterisk symbol (*) are not supported on the conga-E852/855.

Table 17 FDC Signal Descriptions

Signal	Description of FDC signals (shared with LPT)	I/O	PU/PD	Comment
FLPY#	Floppy Interface configuration input	N.A.		Not supported, see section 4.3.5 for more information.
RES	N.C.	N.A.		Not available
DENSEL	Density select: low = 250/300Kb/s high = 500/1000Kb/s	O 5V		
INDEX#	Index signal	I 5V		
TRK0#	Track signal	I 5V		
WP#	Write protect signal	I 5V		
RDATA#	Raw data read	I 5V		
DSKCHG#	Disk change	I 5V		
HSEL#	Head select	O 5V		
DIR#	Direction	O 5V		
STEP#	Motor step	O 5V		
DRV	Drive select	O 5V		
MOT#	Motor select	O 5V		
WDATA#	Raw write data	O 5V		
WGATE#	Write enable	O 5V		

Table 18 Floppy Support Mode Pinout

Floppy Support Mode Pinout			
Pin	Signal	Pin	Signal
51	N.A.	52	RESERVED
53	VCC	54	GND
55	RESERVED	56	DENSEL
57	RESERVED	58	RESERVED
59	IRRX	60	HDSEL#
61	IRTX	62	RESERVED
63	RXD2	64	DIR#
65	GND	66	GND
67	RTS2#	68	RESERVED
69	DTR2#	70	STEP#
71	DCD2#	72	DSKCHG#
73	DSR2#	74	RDATA#
75	CTS2#	76	WP#
77	TXD2	78	TRK0#
79	RI2#	80	INDEX#
81	VCC	82	VCC
83	RXD1	84	DRV
85	RTS1#	86	MOT
87	DTR1#	88	WDATA#
89	DCD1#	90	WGATE#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

Table 19 LPT Signal Descriptions

Signal	Description of LPT signals (shared with FDC)	I/O	PU/PD	Comment
LPT	LPT Interface configuration input	N.A.		Not supported, see section 4.3.5 for more information.
STB#	Strobe signal	O 5V		
AFD#	Automatic feed	O 5V		
PD0	Data bus D0	I/O 5V		
PD1	Data bus D1	I/O 5V		
PD2	Data bus D2	I/O 5V		
PD3	Data bus D3	I/O 5V		
PD4	Data bus D4	I/O 5V		
PD5	Data bus D5	I/O 5V		
PD6	Data bus D6	I/O 5V		
PD7	Data bus D7	I/O 5V		
ERR#	LPT error	I 5V		
INIT#	Initiate	O 5V		
SLIN#	Select	O 5V		
ACK#	Acknowledge	I 5V		
BUSY	Busy	I 5V		
PE	Paper empty	I 5V		
SLCT	Power On	I 5V		

Table 20 LPT Support Mode Pinout

Parallel Port Mode Pinout			
Pin	Signal	Pin	Signal
51	N.A.	52	RESERVED
53	VCC	54	GND
55	STB#	56	AFD#
57	RESERVED	58	PD7
59	IRRX	60	ERR#
61	IRTX	62	PD6
63	RXD2	64	INIT#
65	GND	66	GND
67	RTS2#	68	PD5
69	DTR2#	70	SLIN#
71	DCD2#	72	PD4
73	DSR2#	74	PD3
75	CTS2#	76	PD2
77	TXD2	78	PD1
79	RI2#	80	PD0
81	VCC	82	VCC
83	RXD1	84	ACK#
85	RTS1#	86	BUSY
87	DTR1#	88	PE
89	DCD1#	90	SLCT
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

7.6 X4 Connector Signal Descriptions

Table 21 Signal Descriptions

Signal	Description	I/O	Comment
VCC	Power Supply +5VDC, ±5%	I	external supply
GND	Power Ground	I	external supply
N.C.	Not connected	N.A.	Do not connect
PIDE	Refers to Primary IDE channel	I/O	
SIDE	Refers to Secondary IDE channel	I/O	

Table 22 IDE Signal Descriptions

Signal	Description of IDE signals	I/O	PU/PD	Comment
PIDE_D0..15	Primary IDE Data bus	I/O 3.3V		5V tolerant
PIDE_A0..2	Primary IDE Address bus	O 3.3V		
PIDE_CS1#	Primary IDE chip select channel 0	O 3.3V		
PIDE_CS3#	Primary IDE chip select channel 1	O 3.3V		
PIDE_DRQ	Primary IDE DMA request	I 3.3V		5V tolerant
PIDED_AK#	Primary IDE DMA acknowledge	O 3.3V		
PIDE_RDY	Primary IDE ready	I 3.3V	PU 4k7 3.3V	5V tolerant
PIDE_IOR#	Primary IDE IO read	O 3.3V		
PIDE_IOW#	Primary IDE IO write	O 3.3V		
PIDE_INTRQ	Primary IDE interrupt request	I 3.3V		5V tolerant
SIDE_D0..15	Secondary IDE Data bus	I/O 3.3V		5V tolerant
SIDE_A0..2	Secondary IDE Address bus	O 3.3V		
SIDE_CS1#	Secondary IDE chip select channel0	O 3.3V		
SIDE_CS3#	Secondary IDE chip select channel1	O 3.3V		
SIDE_DRQ	Secondary IDE DMA request	I 3.3V		5V tolerant
SIDED_AK#	Secondary IDE DMA acknowledge	O 3.3V		
SIDE_RDY	Secondary IDE ready	I 3.3V	PU 4k7 3.3V	5V tolerant
SIDE_IOR#	Secondary IDE IO read	O 3.3V		
SIDE_IOW#	Secondary IDE IO write	O 3.3V		
SIDE_INTRQ	Secondary IDE interrupt request	I 3.3V		5V tolerant
DASP_S	Secondary IDE Drive active	O 3.3V		
PDIAG_S	Secondary IDE 80 pin cable detect	I 3.3V	PD 8k2	5V tolerant
HDRST#	Hard Drive reset	O 3.3V		
CBLID_P#	Primary IDE 80pin cable detect	I 3.3V	PD 8k2	5V tolerant

Table 23 Ethernet Signal Descriptions

Signal	Description of Ethernet signals	I/O	PU/PD	Comment
TXD#, TXD	Ethernet transmit signal pair	O		Signals for external transformer
RXD#, RXD	Ethernet receive signal pair	I		Signals for external transformer
ACTLED#	Ethernet activity LED	O 3.3V		
LILED#	Ethernet link LED	O 3.3V		
SPEEDLED#	Ethernet speed LED, ON at 100Mb/s	O 3.3V		

Table 24 Power Control Signals

Signal	Description of Power Control signals	I/O	PU/PD	Comment
PWGIN	Power good input	I	PU 1M 3.3VSB	Also usable as reset input, make low with O.C. to cause reset.
5V_SB	Supply of internal suspend circuit	P		
PS_ON#	ATX Power On	O		
PWRBTN#	Power Button	I	PU 4k7 5VSB	Pull low to switch ATX on

Table 25 Power Management Signals

Signal	Description of Power Management signals	I/O	PU/PD	Comment
RSMRST#	Standby voltage control	I/O 3.3V	PU 10k 3.3VSB	Normally leave open
SMBALRT#	System management bus alert input	I 3.3V	PU 10k 3.3VSB	
BATLOW#	Battery low input	I 3.3V	PU 47k 5VSB	
GPE1#	General purpose power management event input 1	I 3.3V	PU 8k2 3.3VSB	
GPE2#	General purpose power management event input 2	I 3.3V	PU 8k2 3.3VSB	Ring indicator wakeup
EXTSMI#	System management interrupt input	I 3.3V	PU 8k2 3.3VSB	

Table 26 Miscellaneous Signal Descriptions

Signal	Description of Miscellaneous signals	I/O	PU/PD	Comment
SPEAKER	Speaker output	O 3.3V	PU 1k 3.3V	SPEAKER is a boot strap signal (see note below)
BATT	Battery supply	I (2.0 ... 3.6 V)		Power for RTC
I ² CLK	I ² C Bus clock	I/O 5V	PU 4k2 5V	
I ² DAT	I ² C Bus Data	I/O 5V	PU 4k2 5V	
SMBCLK	SM Bus clock	I/O 3.3V	PU 8k2 3.3V	
SMBDATA	SM Bus Data	I/O 3.3V	PU 8k2 3.3V	
KBINH#	Keyboard inhibit	I 5V	PU 47k 5V	
OVCR#	Over current detect for USB	I 3.3V	PU 10k 3.3V	Pull low to generate USB overcurrent event for OS
ROMKBCS#	Do not connect	N.A.		Not available
EXT_PRG	Do not connect	N.A.		Not available
GPCS#	General purpose chip select	N.A.		Not available

 **Note**

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.9 of this User's guide.

7.7 X4 Connector Pinout

Table 27 Connector X4 Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	GND	51	SIDE_IOW#	52	PIDE_IOR#
3	5V_SB	4	PWGIN	53	SIDE_DRQ	54	PIDE_IOW#
5	PS_ON#	6	SPEAKER	55	SIDE_D15	56	PIDE_DRQ
7	PWRBTN#	8	BATT	57	SIDE_D0	58	PIDE_D15
9	KBINH#	10	LILED#	59	SIDE_D14	60	PIDE_D0
11	RSMRST#	12	ACTLED#	61	SIDE_D1	62	PIDE_D14
13	ROMKBCS# (*)	14	SPEEDLED#	63	SIDE_D13	64	PIDE_D1
15	EXT_PRG (*)	16	I2CLK	65	GND	66	GND
17	VCC	18	VCC	67	SIDE_D2	68	PIDE_D13
19	OVCR#	20	GPCS# (*)	69	SIDE_D12	70	PIDE_D2
21	EXTSMI#	22	I2DAT	71	SIDE_D3	72	PIDE_D12
23	SMBCLK	24	SMBDATA	73	SIDE_D11	74	PIDE_D3
25	SIDE_CS3#	26	SMBALRT#	75	SIDE_D4	76	PIDE_D11
27	SIDE_CS1#	28	DASP_S	77	SIDE_D10	78	PIDE_D4
29	SIDE_A2	30	PIDE_CS3#	79	SIDE_D5	80	PIDE_D10
31	SIDE_A0	32	PIDE_CS1#	81	VCC	82	VCC
33	GND	34	GND	83	SIDE_D9	84	PIDE_D5
35	PDIAG_S	36	PIDE_A2	85	SIDE_D6	86	PIDE_D9
37	SIDE_A1	38	PIDE_A0	87	SIDE_D8	88	PIDE_D6
39	SIDE_INTRQ	40	PIDE_A1	89	GPE2#	90	CBLID_P#
41	BATLOW#	42	GPE1#	91	RXD#	92	PIDE_D8
43	SIDE_AK#	44	PIDE_INTRQ	93	RXD	94	SIDE_D7
45	SIDE_RDY	46	PIDE_AK#	95	TXD#	96	PIDE_D7
47	SIDE_IOR#	48	PIDE_RDY	97	TXD	98	HDRST#
49	VCC	50	VCC	99	GND	100	GND

 **Note**

The signals marked with an asterisk symbol () are not supported on the conga-E852/855.*

7.8 DVO Connector X6

Connector and flat foil cable information for the DVO connector (X6) located on the bottom side of the conga-E852/855.



- Connector type Hirose 0.5mm Pitch Bottom Contact Type
Order no. FH12-50S-0.5SH
- FFC type 50 positions, 30cm length, 0.5mm pitch both ends opposite sides
Manufacturer YOUNGSHIN
Order No. MCAB50x300B05

Table 28 DVO Pinout Description

Pin	Signal	Description	PU/PD
1	GND	Ground	
2	DVOC_D0	DVO data signal 0	
3	GND	Ground	
4	VCC5_1	Power supply +5V VCC	
5	DVOC_D1	DVO data signal 1	
6	GND	Ground	
7	DVOC_D2	DVO data signal 2	
8	VCC5_1	Power supply +5V VCC	
9	GND	Ground	
10	DVOC_D3	DVO data signal 3	
11	GND	Ground	
12	GND	Ground	
13	DVOC_D4	DVO data signal 4	
14	GND	Ground	
15	DVOC_D5	DVO data signal 5	
16	GND	Ground	
17	GND	Ground	
18	DVOC_D6	DVO data signal 6	
19	GND	Ground	
20	GND	Ground	
21	DVOC_D7	DVO data signal 7	
22	GND	Ground	
23	DVOC_D8	DVO data signal 8	
24	GND	Ground	
25	GND	Ground	

Pin	Signal	Description	PU/PD
26	DVOC_D9	DVO data signal 9	
27	GND	Ground	
28	GND	Ground	
29	DVOC_D10	DVO data signal 10	
30	GND	Ground	
31	DVOC_D11	DVO data signal 11	
32	GND	Ground	
33	DVOC_CLK	DVO positive clock output signal	
34	DVOC_CLK#	DVO negative clock output signal	
35	GND	Ground	
36	NC1	Not connected	
37	NC2	Not connected	
38	GND	Ground	
39	DVOC_VSYNC	DVO vertical sync signal	
40	DVOC_HSYNC	DVO horizontal sync signal	
41	DVOC_BLANK	DVO blank signal	
42	DVOC_FLDSTL	DVO field stall signal	PD 100k
43	NC3	Not connected	
44	NC4	Not connected	
45	NC5	Not connected	
46	NC6	Not connected	
47	DVO_INTR#	DVO interrupt signal	PU 100k 1.5V
48	MI2C_DAT	MI2C I ² C data line for DVO device	PU 2.2k 1.5V
49	MI2C_CLK	MI2C I ² C clock line for DVO device	PU 2.2k 1.5V
50	DVO_VREF	DVO reference voltage supply	1k/1k voltage divider on 1.5V

7.9 Boot Strap Signals

Table 29 Boot strap signal Descriptions

Signal	Description of Boot Strap Signals	I/O	PU/PD	Comment
DTR1#	PNPVS IO controller	O 5V	PU 4k7 5V	DTR1# is a boot strap signal (see caution statement below)
TXD1	PENKBC IO controller	O 5V	PU 4k7 5V	TXD1 is a boot strap signal (see caution statement below)
TXD2	PEN48 IO controller	O 5V	PU 4k7 5V	TXD2 is a boot strap signal (see caution statement below)
RTS1#	HEFRAS IO controller	O 5V	PD100k	RTS1 is a boot strap signal (see caution statement below)
SPEAKER	TCO Timer disable ICH4	O 3.3V	PU 1k 3.3V	SPEAKER is a boot strap signal (see caution statement below)
BALE	BIOS address range disabled	O 5V	PD 10k	BALE is a boot strap signal (see caution statement below)
AEN	Normal operation	O 5V	PD 10k	AEN is a boot strap signal (see caution statement below)
TC	Disable SMB Boot ROM	O 5V	PD 10k	TC is a boot strap signal (see caution statement below)



Caution

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either ETX[®] internally implemented resistors or chipset internally implemented resistors that are located on the module. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the ETX[®] module to malfunction and/or cause irreparable damage to the module.

If it is necessary to drive a TTL input (or another input which sources or sinks significant current) that uses the TXD1 signal, a CMOS-input buffer can be inserted in the signal path so that this line is not pulled up or down by external circuitry during system reset.

8 System Resources

8.1 System Memory Map

Table 30 Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
(TOM-8MB) – TOM	N.A.	1 or 8MB	VGA frame buffer *
(TOM-8MB-64kB) – (TOM-8MB)	N.A.	64kB	ACPI reclaim and NVS area **
1024kB – (TOM-8MB-64kB)	100000 – N.A	N.A.	Extended memory
869kB – 1024kB	E0000 - FFFFF	128kB	Runtime BIOS
800kB – 869kB	CC000 - DFFFF	96kB	Upper Memory
640kB – 800kB	A0000 - CBFFF	160kB	Video memory and BIOS
639kB – 640kB	9FC00 - 9FFFF	1kB	Extended BIOS data
512kB – 639kB	80000 - 9FC00	127kB	Extended conventional memory.
0 – 512kB	00000 - 7FFFF	512kB	Conventional memory

Notes

1. *T.O.M. = Top of memory = max. DRAM installed*
2. ** VGA frame buffer can be reduced to 1MB in setup.*
3. *** Only if ACPI Aware OS is set to YES in setup.*

8.2 I/O Address Assignment

The I/O address assignment of the conga-E852/855 module is functionally identical with a standard PC/AT. The most important addresses and the ones that differ from the standard PC/AT configuration are listed in the table below.

Table 31 I/O Address Assignment

I/O Address (hex)	Size	Available	Description
0000 - 00FF	256 bytes	No	Motherboard resources
0100 - 010F	16 bytes	No	congatec System Control
0170 - 0177	8 bytes	No	Secondary IDE channel
01F0 - 01F7	8 bytes	No	Primary IDE channels
0278 - 027F	8 bytes	Note 2	Parallel Port 2 (LPT2)
02E8 - 02EF	8 bytes	Note 2	Serial Port 4 (COM4)
02F8 - 02FF	8 bytes	Note 1	Serial Port 2 (COM2)
0376	1 byte	No	Secondary IDE channel command port
0377	1 byte	No	Secondary IDE channel status port
0378 - 037F	8 bytes	Note 1	Parallel Port 1 (LPT1)
03B0 - 03DF	16 bytes	No	Video system
03E8 - 03EF	8 bytes	Note 2	Serial Port 3 (COM3)
03F0 - 03F5	6 bytes	No	Floppy channel 1
03F6	1 byte	No	Primary IDE channel command port
03F7	1 byte	No	Primary IDE channel status port
03F8 - 03FF	8 bytes	Note 1	Serial Port 1 (COM1)
0CF8 - 0CFB	4 bytes	No	PCI configuration address register
0CFC - 0CFF	4 bytes	No	PCI configuration data register
0480 - 04BF	64 bytes	No	Motherboard resources
04D0 - 04D1	2 bytes	No	Motherboard resources
0800 - 087F	128 bytes	No	Motherboard resources
0A00 - 0A0F	16 bytes	No	Motherboard resources
0800 - 087F	128 bytes	No	Motherboard resources
0D00 - FFFF		Note 3	PCI Bus

Notes

1. Default, but can be changed to another address range.
2. When baseboard external Super I/O controller is present.
3. The BIOS assigns PCI I/O resources from FFF0h downwards. Non PnP/PCI compliant devices must not consume I/O resources in that area.

8.3 Interrupt Request (IRQ) Lines

Table 32 **IRQ Lines in PIC mode**

IRQ#	Available	Typical Interrupt Source	Connected to Pin
0	No	Counter 0	N.A.
1	No	Keyboard	N.A.
2	No	cascade interrupt from slave PIC	N.A.
3	Note 1	Serial Port 1 (COM1) / Generic	IRQ3
4	Note 1	Serial Port 2 (COM2) / Generic	IRQ4
5	Note 2	Parallel Port 2 (LPT2) / Generic	IRQ5
6	Note 1	Floppy Drive Controller / Generic	IRQ6
7	Note 1	Parallel Port 1 (LPT1) / Generic	IRQ7
8	No	Real-time Clock	N.A.
9	Note 4	SCI / Generic	IRQ9
10	Note 2	Serial Port 3 (COM3) / Generic	IRQ10
11	Note 2	Serial Port 4 (COM4) / Generic	IRQ11
12	Note 1	PS/2 Mouse / Generic	IRQ12
13	No	Math processor	N.A.
14	Note 1, 3	IDE Controller 0 (IDE0) / Generic	IRQ14
15	Note 1, 3	IDE Controller 1 (IDE1) / Generic	IRQ15

In PIC mode, the PCI Bus interrupt lines can be routed to any free IRQ.

Notes

- 1. Default, but can be changed to another address range. If disabled in BIOS setup resource can be used for another purpose.*
- 2. Function described is available if the baseboard is equipped with the I/O controller SMSC669. This I/O controller is supported by the congatec Embedded BIOS.*
- 3. If the IDE controller is set to native IDE mode, IRQ14 and 15 are free for PCI/ISA Bus.*
- 4. In ACPI mode, IRQ9 is used for the SCI (System Control Interrupt). The SCI can be shared with a PCI interrupt line.*

Table 33 IRQ Lines in APIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin / Function
0	No	Counter 0	N.A.
1	No	Keyboard	N.A.
2	No	cascade interrupt from slave PIC	N.A.
3	Note 1	Serial Port 1 (COM1) / Generic	IRQ3
4	Note 1	Serial Port 2 (COM2) / Generic	IRQ4
5	Note 2	Parallel Port 2 (LPT2) / Generic	IRQ5
6	Note 1	Floppy Drive Controller / Generic	IRQ6
7	Note 1	Parallel Port 1 (LPT1) / Generic	IRQ7
8	No	Real-time Clock	N.A.
9	Note 4	Generic	IRQ9, Option for SCI
10	Note 2	Serial Port 3 (COM3) / Generic	IRQ10
11	Note 2	Serial Port 4 (COM4) / Generic	IRQ11
12	Note 1	PS/2 Mouse / Generic	IRQ12
13	No	Math processor	N.A.
14	Note 1, 3	IDE Controller 0 (IDE0) / Generic	IRQ14
15	Note 1, 3	IDE Controller 1 (IDE1) / Generic	IRQ15
16	No	N.A.	UHCI host controller 1, VGA controller
17	Yes	N.A.	PCI Bus INTD, AC97 Audio, SMBus host controller
18	No	N.A.	IDE controller (native mode)
19	Yes	N.A.	PCI Bus INTC
20	No	N.A.	Onboard LAN controller, Option for SCI
21	Yes	N.A.	PCI Bus INTA
22	Yes	N.A.	PCI Bus INTB
23	No	N.A.	EHCI host controller

In APIC mode, the PCI Bus interrupt lines are internally routed to IRQ17, 19, 21 and 22.


Notes

1. Default but can be changed to another address range. If disabled in BIOS setup resource can be used for another purpose.
2. Function described is available if the baseboard is equipped with the I/O controller SMSC669. This I/O controller is supported by the congatec Embedded BIOS.
3. If the IDE controller is set to native IDE mode, IRQ14 and 15 are free for PCI/ISA Bus.
4. In ACPI mode, IRQ9 is used for the SCI (System Control Interrupt). The SCI can be shared with a PCI interrupt line.

8.4 Direct Memory Access (DMA) Channels

Table 34 DMA Channels

DMA#	Data Width	Available	Description
0	8 or 16 bits	Yes	
1	8 or 16 bits	Yes	
2	8 or 16 bits	Note 1	Floppy Drive Controller
3	8 or 16 bits	Note 2	Parallel Port (LPT)
4	8 or 16 bits	No	Cascade DMA Controller
5	16 bits	Yes	
6	16 bits	Yes	
7	16 bits	Yes	

Notes

- 1. If the corresponding device is disabled in BIOS setup then the DMA channel can be used by customers hardware.*
- 2. Not available if Parallel Port is used in ECP mode (Enhanced Parallel Port).*

8.5 PCI Configuration Space Map

Table 35 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	00h	00h	N.A.	Host Bridge
00h	02h	00h	Internal	VGA Graphics
00h	1Dh	00h	Internal	UHCI Host Controller 1
00h	1Dh	01h	Internal	UHCI Host Controller 2
00h	1Dh	07h	Internal	EHCI Host Controller
00h	1Eh	00h	Internal	PCI to PCI Bridge
00h	1Fh	00h	N.A.	PCI to LPC Bridge
00h	1Fh	01h	Internal	IDE Controller
00h	1Fh	03h	Internal	SMBus Host Controller
00h	1Fh	05h	Internal	AC97 Audio Controller
01h	08h	00h	Internal	Onboard LAN Controller
01h	03h	xxh	INTA-INTD	PCI Bus Slot 1
01h	04h	xxh	INTA-INTD	PCI Bus Slot 2
01h	05h	xxh	INTA-INTD	PCI Bus Slot 3
01h	06h	xxh	INTA-INTD	PCI Bus Slot 4

8.6 PCI Interrupt Routing Map

Table 36 PCI Interrupt Routing Map

PIRQ	PCI Bus INT line (see note below)	VGA	UHCI 1	UHCI 2	EHCI	IDE native	SM Bus	AC97	LAN
A		x	x						
B	INTD						x	x	
C						x			
D	INTC			x					
E									x
F	INTA								
G	INTB								
H					x				

 **Note**

These interrupts are available for external devices/slots via the X1 connector.

8.7 PCI Bus Masters

The conga-E852/855 supports 4 external PCI Bus Masters. There are no limitations in connecting bus master PCI devices.

 **Note**

If there are two devices connected to the same PCI REQ/GNT pair and they are transferring data at the same time then the latency time of these shared PCI devices can not be guaranteed.

8.8 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

8.9 SM Bus

System Management (SM) bus signals are connected to the Intel[®] ICH4 82801DB and the SMBus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

9 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

9.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the key during POST.

9.1.1 Boot Selection Popup

The BIOS offers the possibility to access a Boot Selection Popup menu by pressing the <F11> key during POST. If this option is used a message will be displayed during POST stating that the “Boot Selection Popup menu has been selected” and the menu itself will be displayed immediately after POST thereby allowing the operator to choose the boot device to be used.

9.1.2 Manufacturer Default Settings

Pressing the <End> key repeatedly, immediately after power is initiated will result in the manufacturer default settings being loaded for that boot sequence and only that boot sequence. This is helpful when a previous BIOS setting is no longer desired. If you want to change the BIOS settings, or save the manufacturer default settings, then you must enter the BIOS setup program and use the 'Save and Exit' function. This feature is enabled by default. See setup node in the “BIOS Setup Program” section 9.6.1 “Security Settings”.

9.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar and two main frames. The menu bar is shown below:

 **Note**

Entries in the option column that are displayed in bold print indicate BIOS default values.

Main	Advanced	Boot	Security	Power	Exit
------	----------	------	----------	-------	------

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2/F3	Change Colors of setup screen.
F7	Discard Changes.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter sub menu.

9.3 Main Setup

When you first enter the BIOS setup, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab.

The Main screen reports BIOS, processor, memory and board information and is for configuring the system date and time.

Feature	Options	Description
System Time	Hour:Minute:Second	Specifies the current time. <i>Note: The time is in 24-hour format.</i>
System Date	Day of week, month/day/year	Specifies the current date. <i>Note: The date is in month-day-year format.</i>
BIOS ID	no option	Displays the BIOS ID.
Processor	no option	Displays the processor type and frequency.
System Memory	no option	Displays the total amount of system memory.
Product Revision	no option	Displays the hardware revision of the board.
Serial Number	no option	Displays the serial number of the board.
BC Firmware Rev.	no option	Displays the revision of the congatec board controller.
MAC Address	no option	Displays the MAC address of the onboard Ethernet controller
Boot Counter	no option	Displays the number of boot-ups (max. 16777215).
Running Time	no option	Displays the time the board is running [in h] (max. 65535).

9.4 Advanced Setup

Select the Advanced tab from the setup menu to enter the Advanced BIOS Setup screen. The menu is used for setting advanced features:

Main	Advanced	Boot	Security	Power	Exit
	ACPI Configuration				
	PCI Configuration				
	Graphics Configuration				
	CPU Configuration				
	Chipset Configuration				
	I/O Interface Configuration				
	Clock Configuration				
	IDE Configuration				
	USB Configuration				
	Keyboard/Mouse Configuration				
	Remote Access Configuration				
	Hardware Health Configuration				
	Watchdog Configuration				

9.4.1 ACPI Configuration Submenu

Feature	Options	Description
ACPI Aware O/S	No Yes	Set this value to allow the system to utilize the Intel ACPI (Advanced Configuration and Power Interface). Set to <i>NO</i> for non ACPI aware operating system like DOS and Windows NT. Set to <i>YES</i> if your OS complies with the ACPI specification (e.g. Windows 98, 2000, XP)
ACPI 2.0 Features	No Yes	Enables ACPI 2.0 specific 64-bit pointers in ACPI tables.
ACPI APIC support	Enabled Disabled	Set to enable to include the APIC support table to ACPI.
Active Cooling Trip Point	Disabled 50, 60, 70, 80, 90°C	Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off.
Passive Cooling Trip Point	Disabled 50, 60, 70, 80, 90 °C	Specifies the temperature threshold at which the ACPI aware OS starts/stops CPU clock throttling.
Critical Trip Point	Disabled, 80, 85, 90, 95, 100, 105 , 110°C	Specifies the temperature threshold at which the ACPI aware OS performs a critical shutdown.
Watchdog ACPI Event	Shutdown Restart	Selects the event that is initiated by the watchdog ACPI event (see note below).
GPE1 Function	No Function Lid Switch	Determines the functionality of GPE1 (pin 42 of X4)
GPE2 Function	No Function Sleep Button	Determines the functionality of GPE2 (pin 89 of X4)

Note

In ACPI mode it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

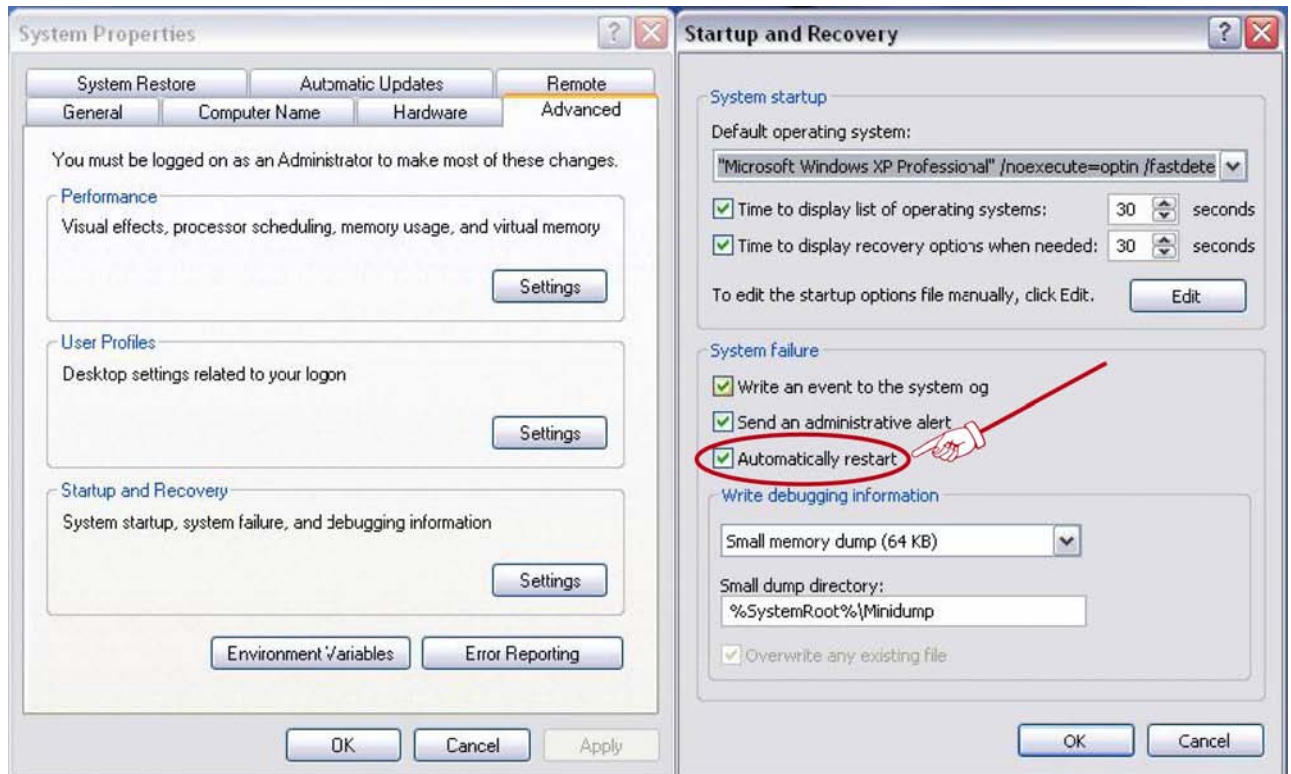
For Restart: An ACPI fatal error is reported to the OS.

It depends on your particular OS as to how this reported fatal error will be handled when the Restart function is selected. If you are using Windows XP/2000 there is a setting that can be enabled to ensure that the OS will perform a restart when a fatal error is detected. After a very brief blue-screen the system will restart.

You can enable this setting buy going to the "System Properties" dialog box and choosing the "Advanced" tab. Once there choose the "Settings" button for the "Startup and Recovery" section. This will open the "Startup and Recovery" dialog box. In this dialog box under "System failure" there are three check boxes that define what Windows will do when a fatal error has been detected. In order to ensure that the system restarts after a 'Watchdog ACPI Event' that is set to 'Restart', you must make sure that the check box for the selection "Automatically restart" has been checked. If this option is not selected then Windows will remain at a blue-screen after a 'Watchdog

ACPI Event" that has been configured for 'Restart' has been generated. The following page has a Windows screen-shot showing the proper configuration.

Win XP/2000 Watchdog ACPI Event restart configuration



9.4.2 PCI Configuration Submenu

Feature	Options	Description
Plug & Play O/S	No Yes	Specifies if manual configuration is desired. Set to <i>NO</i> for operating systems that do not meet the Plug and Play specification. In this case the BIOS configures all devices in the system. Select <i>YES</i> to let the operating system configure PnP devices that are not required for booting.
PCI Latency Timer	32, 64 , 96, ... 248	This option allows you to adjust the latency timer of all devices on the PCI bus.
Allocate IRQ to PCI VGA	Yes No	Allow or restrict the BIOS from giving the VGA controller an IRQ resource.
Allocate IRQ to SMBUS HC	Yes No	Allow or restrict the BIOS from giving the SMBus host controller an IRQ resource.
▶ PCI IRQ Resource Exclusion	sub menu	Opens PCI IRQ Resource Exclusion sub menu.
▶ PCI Interrupt Routing	sub menu	Opens PCI Interrupt Routing sub menu.

9.4.2.1 PCI IRQ Resource Exclusion Submenu

Feature	Options	Description
IRQ xx	Available Reserved	Allow or restrict the BIOS from giving IRQ resource to PCI/PNP devices. <i>Note: Assigned IRQ resources are shaded and listed as 'Allocated'.</i>

9.4.2.2 PCI Interrupt Routing Submenu

Feature	Options	Description
PIRQ xx (devices)	Auto , 3, 4, ..., 14, 15	Select fixed IRQ for PCI interrupt line or set to AUTO to let the BIOS and operating system route an IRQ. <i>Note: Only those IRQs that are free are listed.</i>

9.4.3 Graphics Configuration Submenu

Feature	Options	Description
Primary Video Device	Internal VGA PCI /Int.VGA	Select primary video adapter to be used during during boot up.
Graphics Mode Select	Disabled Enabled, 1MB Enabled, 4MB Enabled, 8MB Enabled, 16MB Enabled, 32MB	This option allows you to disable the onboard video controller or enable it with 1MB to max. 32MB frame buffer size.
Graphics Engine 2	Disabled Enabled	Enables the 2nd graphics engine for dual independent display support.
Primary Boot Display	LFP=LVDS EFP=DVO	Select the primary display if LFP and EFP are connected. Only one of them can be enabled during BIOS boot-up.
Graphics Aperture Size	64MB 128MB 256MB	Sets the aperture size for the video controller.
Boot Display Device	Auto CRT only EFP only CRT + EFP LFP only CRT + LFP	Select the display device used for boot up. EFP = Digital Flat Panel (DVO) Auto uses VGA BIOS defaults. <i>Note: If a DFP and a LFP are connected, the VGA BIOS enables the EFP by default.</i>
Flat Panel Type	Auto VGA 1x18 (002h) VGA 1x18 (013h) SVGA 1x18 (004h) XGA 1x18 (006h) XGA 2x18 (007h) XGA 1x24 (008h) XGA 2x24 (012h) SXGA 2x24 (00Ah) UXGA 2x24 (00Ch) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or set to AUTO to let the BIOS auto detect the attached LVDS panel. Auto detection is performed by reading an EDID™ data set via the panel DDC bus. <i>Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.</i> VGA = 640x480 SVGA = 800x600 XGA = 1024x768 SXGA = 1280x1024 UXGA = 1600x1200
Local Flat Panel Scaling	Centering Expand Text Expand Graphics Expand Text & Graphics	Select whether and how to scale the actual video mode resolution to the local flat panel resolution.
Backlight Control	0%, 25%, 50%, 75%, 100%	Set local flat panel backlight control value.

9.4.4 CPU Configuration Submenu

Feature	Options	Description
Processor Info Block	no option	Displays the processor manufacturer, brand, frequency, and cache sizes.
Intel SpeedStep tech	Maximum Speed Minimum Speed Automatic Disabled	Maximum: CPU speed is set to maximum. Minimum: CPU speed is set to minimum. Automatic: CPU speed is controlled by the operating system. Disabled: No Speedstep, default CPU speed. <i>Note: This option is not available for Celeron M CPUs</i>
Max. CPU Frequency	(Available options depend on processor)	Allows to reduce the maximum processor frequency. This limits the maximum frequency the CPU can be set to when SpeedStep is set to Automatic or Maximum Speed. <i>Note: This option is not available for Celeron M CPUs and is only visible if Intel SpeedStep Tech is set to Automatic or Maximum Speed.</i>
On Demand Clock Modulation	Disabled 75% 50% 25%	Allows a reduction of the performance of the processor by utilizing clock modulation. The value indicates the CLOCK ON to CLOCK OFF interval ratio. E.g. 75% results in a performance decrease of about 25%. <i>Note: This option is only available for Celeron M CPUs</i>
Execute Disable Bit	Disabled Enabled	When disabled force the XD feature flag to always return to 0.

9.4.5 Chipset Configuration Submenu

Feature	Options	Description
Memory Hole	Disabled 15MB-16MB	Enables a 1MB memory hole for ISA bus access at address 15MB.
C000, 16k Shadow	Disabled Uncached Write Protect Cached Write Trough Cached Write Back Cached	Select the type of shadow and cache scheme to be used for this memory region.
C400, 16k Shadow	see above	see above
C800, 16k Shadow	see above	see above
CC00, 16k Shadow	see above	see above
D000, 16k Shadow	see above	see above
D400, 16k Shadow	see above	see above
D800, 16k Shadow	see above	see above
DC00, 16k Shadow	see above	see above
IOAPCI	Disabled Enabled	Enable internal IO(x) APIC and its address decode.
APIC ACPI SCI IRQ	Disabled Enabled	Only displayed and valid if the IOAPIC is enabled! If set to Disabled IRQ9 is used for the SCI. If set to Enabled IRQ20 is used for the SCI.

9.4.6 I/O Interface Configuration Submenu

Feature	Options	Description
OnBoard AC97 Audio	Auto Disabled	Disable the ICH4 AC'97 audio controller function. Auto enables the audio controller if a codec is mounted.
OnBoard LAN	Disabled Enabled	Enable / Disable the ICH4 onboard LAN controller.
Onboard Floppy Controller	Disabled Enabled	Enable / Disable the onboard floppy controller.
Floppy A	Disabled 360 KB 5¼" 1.2 MB 5¼" 720 KB 3 ½" 1.44 MB 3 ½" 2.88 MB 3 ½"	Select the floppy drive A type.
Serial Port 1/2 Address	Disabled 3F8/IRQ4 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Specifies the I/O base address and IRQ of serial port 1/2.
Serial Port 2 Mode	Normal IrDA ASK IR	Specifies the mode for serial port 2.
IR Duplex Mode	Full Duplex Half Duplex	Select IRDA full or half duplex function.
IR I/O Pin Select	SINB/SOUTB IRRX/RTX	Select receiver and transmit pins for IRDA mode.
Parallel Port Address	Disabled 378 278 3BC	Specifies the I/O base address used by the parallel port.
Parallel Port Mode	Normal Bi-directional ECP EPP ECP&EPP	Specifies the parallel port mode.
EPP Version	1.9 1.7	Specifies the EPP version.
Parallel Port DMA	DMA0 DMA1 DMA3	Specifies the DMA channel for parallel port in ECP mode.
Parallel Port IRQ	None IRQ5 IRQ7	Specifies the interrupt for the parallel port.
External Floppy Controller	Disabled Enabled	Enable / Disable the external floppy controller. (see note below)
Serial Port 3 Configuration	Disabled Enabled	Enable / Disable the external Serial Port 3. (see note below)
Base Address	3F8h, 2F8h, 3E8h , 2E8h	Set the I/O base address for the serial port 3. (see note below)
Interrupt	IRQ10 , IRQ11	Set the IRQ for the serial port 3. (see note below)

Feature	Options	Description
Serial Port 4 Configuration	Disabled Enabled	Enable / Disable the external Serial Port 4 (see note below)
Base Address	3F8h, 2F8h, 3E8h , 2E8h	Set the I/O base address for the serial port 4 (see note below)
Interrupt	IRQ10, IRQ11	Set the IRQ for the serial port 4. (see note below)
External Parallel Port	Disabled Enabled	Enable / Disable the external parallel Port. (see note below)
Base Address	378h, 278h , 3BCh	Set the I/O base address for the external parallel port. (see note below)
External Parallel Port Mode	Normal Bi-directional EPP	Specifies the parallel port mode. (see note below)
Interrupt	None IRQ5 IRQ7	Specifies the interrupt for the parallel port. (see note below)

 **Note**

The options for external floppy controller, serial port 3, 4 and external parallel port are only visible if a SMSC669 super I/O is mounted on the baseboard.

9.4.7 Clock Configuration

Feature	Options	Description
Spread Spectrum	Disabled Enabled	Enable spread spectrum clock modulation to reduce EMI.
Unused PCI Slot Clocks	Disabled Enabled	Set to disable if you want the BIOS to switch off PCI clocks for non-populated slots.

9.4.8 IDE Configuration Submenu

Feature	Options	Description
Onboard PCI IDE Controller	Disabled Primary Secondary Both	Enables the IDE channels of the integrated IDE controller.
Onboard PCI IDE Operate Mode	Legacy Mode Native Mode	<i>Note: Make sure your OS supports Native IDE mode.</i>
▶ Primary IDE Master	sub menu	Reports type of connected IDE device.
▶ Primary IDE Slave	sub menu	Reports type of connected IDE device.
▶ Secondary IDE Master	sub menu	Reports type of connected IDE device.
▶ Secondary IDE Slave	sub menu	Reports type of connected IDE device.
Hard Disk Write Protect	Disabled Enabled	If enabled, protects the hard drive from being erased. Disabled allows the hard drive to be used normally. Read, write and erase functions can be performed to the disk.
IDE Detect Time Out (s)	0, 5, 10, ... 30, 35	Set this option to stop the BIOS from searching for IDE devices within the specified number of seconds. Basically, this allows you to fine-tune the settings to allow for faster boot times. Adjust this setting until a suitable timing can be found that will allow for all IDE disk drives that are attached to be detected.
ATA(PI) 80Pin Cable Detection	Host&Device Host Device	Select the mechanism for detecting 80Pin ATA(PI) cable. <i>Note: The use of an 80-conductor ATA cable is mandatory for running UDMA66 and faster hard disk drives. The standard 40-conductor ATA cable cannot handle the higher speeds.</i>

9.4.8.1 Primary/Secondary IDE Master/Slave Submenu

Feature	Options	Description
Device	Hard Disk ATAPI CDROM	Displays the type of drive detected. The 'grayed-out' items below are the IDE disk drive parameters taken from the firmware of the IDE disk
Vendor	no option	Manufacturer of the device.
Size	no option	Total size of the device.
LBA Mode	supported not supported	Shows whether the device supports Logical Block Addressing.
Block Mode	number of sectors	Block mode boosts IDE performance by increasing the amount of data transferred. Only 512 byte of data can be transferred per interrupt if block mode is not used. Block mode allows transfers of up to 64 kB per interrupt.
PIO Mode	0, 1, 2, 3, 4	IDE PIO mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases.
Async DMA	no option	This indicates the highest Asynchronous DMA Mode that is supported.
Ultra DMA	no option	This indicates the highest Synchronous DMA Mode that is supported.
S.M.A.R.T	no option	Self-Monitoring Analysis and Reporting Technology protocol used by IDE drives of some manufacturers to predict drive failures.
Type	Not Installed Auto CD/DVD ARMD	Sets the type of device that the BIOS attempts to boot from after the POST has completed. <i>Not Installed</i> prevents the BIOS from searching for an IDE disk. <i>Auto</i> allows the BIOS to auto detect the IDE disk drive type. <i>CD/DVD</i> specifies that an IDE CD/DVD drive is attached. The BIOS will not attempt to search for other types of IDE disk drives. <i>ARMD</i> specifies an ATAPI Removable Media Device. This includes, but is not limited to ZIP and LS-120.
LBA/Large Mode	Disabled Auto	Set to <i>AUTO</i> to let the BIOS auto detect LBA mode control. Set to Disabled to prevent the BIOS from using LBA mode.
Block (Multi-Sector Transfer)	Disabled Auto	Set to <i>AUTO</i> to let the BIOS auto detect device support for multi sector transfer. The data transfer to and from the device will occur multiple (the number of sectors, see above) sectors at a time. Set to Disabled to prevent the BIOS from using block mode. The data transfer to and from the device will occur one sector at a time.
PIO Mode	Auto 0, 1, 2, 3, 4	Set to <i>AUTO</i> to let the BIOS auto detect the supported PIO mode.
DMA Mode	Auto SWDMA0, 1, 2 MWDMA0, 1, 2 UDMA0, 1, 2, 3, 4, 5, 6	Set to <i>AUTO</i> to let the BIOS auto detect the supported DMA mode. SWDMA = Single Word DMA MWDMA = Multi Word DMA UDMA = Ultra DMA
S.M.A.R.T	Auto Disabled Enabled	Set to <i>AUTO</i> to let the BIOS auto detect hard disk drive support. Set to <i>Disabled</i> to prevent the BIOS from using SMART feature. Set to <i>Enabled</i> to allow the BIOS to use SMART feature on supported hard disk drives.
32Bit Data Transfer	Disabled Enabled	Enable/Disable 32-bit data transfers on supported hard disk drives.
ARMD Emulation Type	Auto Floppy Hard disk drive	ARMD is a device that uses removable media, such as the LS120, MO (Magneto-optical), or Iomega Zip drives. If you want to boot from media on ARMD, it is required that you emulate boot up from a floppy or hard disk drive. This is essentially necessary when trying to boot to DOS. You can select the type of emulation used if you are booting such a device.

9.4.9 USB Configuration Submenu

Feature	Options	Description
USB Function	Disabled 2 USB Ports 4 USB Ports	Disable ICH4 USB host controllers. Enable UHCI host controller 1. Enable UHCI host controller 1 + 2.
Legacy USB Support	Disabled Enabled Auto	Legacy USB Support refers to the USB keyboard, USB mouse and USB mass storage device support. If this option is <i>Disabled</i> , any attached USB device will not become available until a USB compatible operating system is booted. However, legacy support for USB keyboard will be present during POST. When this option is <i>Enabled</i> , those USB devices can control the system even when there is no USB driver loaded. <i>AUTO</i> disables legacy support if no USB devices are connected.
USB Keyboard Legacy Support	Disabled Enabled	Enable/Disable USB keyboard legacy support. <i>NOTE: This option has to be used with caution. If the system is equipped with USB keyboard only then the user cannot enter setup to enable the option back.</i>
USB Mouse Legacy Support	Disabled Enabled	Enable/Disable USB mouse legacy support.
USB Storage Device Support	Disabled Enabled	Enable/Disable USB mass storage device support.
Port 64/60 Emulation	Disabled Enabled	Enable/Disable the "Port 60h/64h" trapping option. Port 60h/64h trapping allows the BIOS to provide full PS/2 based legacy support for USB keyboard and mouse. It provides the PS/2 functionalities such as keyboard lock, password setting, scan code selection etc. to USB keyboards.
USB 2.0 Controller	Enabled Disabled	Enable the ICH4 USB 2.0 (EHCI) host controller.
USB 2.0 Controller Mode	FullSpeed HiSpeed	Configures the USB 2.0 host controller in HiSpeed (480Mbps) or FullSpeed (12Mbps).
USB Beep Message	Disabled Enabled	Enable/Disable the beep during USB device enumeration.
BIOS EHCI Hand-Off	Disabled Enabled	Enable workaround for OSes without EHCI hand-off support.
USB Stick Default Emulation	Auto Hard Disk	Select default USB stick emulation type. Auto selects floppy or hard disk emulation based on the storage size of the USB stick, but the emulation type can be manually reconfigured for each device using the Mass Storage Device Configuration sub menu.
USB Mass Storage Reset Delay	10 Sec 20 Sec 30 Sec 40 Sec	Number of seconds the legacy USB support BIOS routine waits for the USB mass storage device after the start unit command.
► USB Mass Storage Device Configuration	sub menu	Opens sub menu. Note: Only visible if USB Stick Default Emulation is set to Auto.

9.4.9.1 USB Mass Storage Device Configuration Submenu

Feature	Options	Description
Emulation Type	Auto Floppy Forced FDD Hard Disk CDROM	<p>Every USB MSD that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device.</p> <p><i>Note: The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly.</i></p> <p>Select <i>AUTO</i> to let the BIOS auto detect the current formatted media.</p> <p>If Floppy is selected then the device will be emulated as a floppy drive.</p> <p><i>Forced FDD</i> allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32.</p> <p><i>Hard Disk</i> allows the device to be emulated as hard disk.</p> <p><i>CDROM</i> assumes the CD-ROM is formatted as bootable media, specified by the 'El Torito' Format Specification.</p>

9.4.10 Keyboard/Mouse Configuration Submenu

Feature	Options	Description
Bootup Num-Lock	Off On	<p>Specifies the power-on state of the Num-lock feature on the numeric keypad of the keyboard.</p>
Typematic Rate	Slow Fast	<p>Specifies the rate at which the computer repeats a key that is held down.</p> <p><i>Slow</i> sets a rate of under 8 times per second.</p> <p><i>Fast</i> sets a rate of over 20 times per second.</p>
PS/2 Mouse Support	Disabled Enabled Auto	<p><i>Disabled</i> will prevent the PS/2 mouse port from using system resources and will prevent the port from being active.</p> <p><i>Enabled</i> activates the PS/2 port and the BIOS offers PS/2 mouse support. Use this setting if you always need PS/2 mouse support even when the mouse is not connected at boot-up time.</p> <p><i>Auto</i> lets the BIOS check for a connected PS/2 mouse and enable support if one is connected.</p>

9.4.11 Remote Access Configuration Submenu

Feature	Options	Description
Remote Access	Disabled Enabled	Enable/Disable the BIOS remote access feature. <i>Note: If the systems serial ports are disabled in the 'I/O Interface Configuration' submenu, then Serial Redirection is disabled and 'Remote Access Configuration' menu is unavailable to the user.</i>
Serial Port Number	COM1 COM2	Select the serial port you want to use for console redirection. <i>Note: Only enabled serial ports are presented as an option.</i>
Serial Port Mode	115200 8,n,1 57600 8,n,1 38400 8,n,1 19200 8,n,1 09600 8,n,1	Select the baud rate (transmitted bits per second) you want the serial port to use for console redirection. <i>Note: The terminal program used with Serial Redirection must be set to use the exact same set of communication parameters.</i>
Flow Control	None Hardware Software	Select the flow control for Serial Redirection.
Redirection After BIOS POST	Disabled Boot Loader Always	With <i>Disabled</i> Serial Redirection functionality is disabled at the end of BIOS POST. If set to <i>Always</i> , all resources and interrupts associated with Serial Redirection are protected and not released to DOS. This option lets Serial Redirection permanently reside at base memory which allows the DOS console to be redirected. <i>Note, that graphics output (VGA, SVGA, etc) from DOS programs is not redirected.</i> If set to <i>Boot loader</i> , Serial Redirection is active during the OS boot loader process. This allows boot status messages to be redirected, but Serial Redirection will terminate when the OS loads.
Terminal Type	ANSI VT100 VT-UTF8	Select the target terminal type. Escape sequences representing keystrokes are sent to the remote terminal based on these settings.
VT-UTF8 Combination Key Support	Disabled Enabled	This option enables VT-UFT8 combination key support for ANSI/VT100 terminals.
Serdir Memory Display Delay	No Delay Delay 1 Sec Delay 2 Sec Delay 4 Sec	Sets the delay in seconds to display the memory information.
Serial Port BIOS Update	Disabled Enabled	Enable/Disable possibility to perform a BIOS update from a host PC connected by a null modem cable on the serial port 1. Disabling this features reduces boot time.

9.4.12 Hardware Monitoring Submenu

Feature	Options	Description
H/W Health Function	Disabled Enabled	Enable hardware health monitoring device and display the readings.
Board Temperature	no option	Current board temperature.
CPU Temperature	no option	Current processor die temperature.
FAN Speed	no option	Current FAN speed.
VcoreA	no option	Current Core A reading.
VcoreB	no option	Current Core B reading.
+3.3Vin	no option	Current 3.3V reading.
+5Vin	no option	Current 5V reading.
VBAT	no option	Current VBAT reading.

9.4.13 Watchdog Configuration Submenu

Feature	Options	Description
POST Watchdog	Disabled 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during bootup by performing a reset.
Runtime Watchdog	Disabled One time trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to ' <i>One time trigger</i> ' the watchdog will be disabled after the first trigger. If set to ' <i>Single event</i> ', every stage will be executed only once, then the watchdog will be disabled. If set to ' <i>Repeated event</i> ' the last stage will be executed repeatedly until a reset occurs.
Delay	see Post Watchdog	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 1 is reached. For more information about <i>ACPI Event</i> see section 9.4.1 of this user's guide.
Event 2	Disabled NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached.
Event 3	Disabled NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached.
Timeout 1	0.5sec 1sec 2sec 5sec 10sec 30sec 1min 2min	Selects the timeout value for the first stage watchdog event.
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.

9.5 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen.

In the upper part of the screen the Boot setup allows you to prioritize the available boot devices. The lower part of this setup screen shows options related to the BIOS boot.

9.5.1 Boot Device Priority

Feature	Options	Description
Boot Priority Selection	Device Based Type Based	Select between device and type based boot priority lists. The "Device Based" boot priority list allows you to select from a list of currently detected devices only. The "Type Based" boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the "Device Based" boot priority list might change dynamically in cases when devices are physically removed or added to the system. The "Type Based" boot menu is static and can only be changed by the user.
1st, 2nd, 3rd, ... Boot Device	Available boot devices Disabled Primary Master Primary Slave Secondary Master Secondary Slave	Select the boot device for 1st, 2nd, ... boot device. The BIOS will try to boot from these devices with the respective priority. This view is only available when in the default "Type Based" mode.
(Up to 12 boot devices can be prioritized if device based priority list control is selected. If "Type Based" priority list control is enabled only 8 boot devices can be prioritized.)	Legacy Floppy USB Harddisk USB CDROM USB Removable Dev. Onboard LAN External LAN PCI Mass Storage PCI SCSI Card Any PCI BEV Device Onboard PCI SATA	When in "Device Based" mode you will only see the devices that are currently connected to the system. The default boot priority is <i>Removables 1st, ATAPI CDROM 2nd, Hard Disk 3rd, BEV 4th</i> (BEV = Boot Entry Vector, e.g. Network or SCSI Option-ROMs).

9.5.2 Boot Device Priority

Feature	Options	Description
Quick Boot	Disabled Enabled	If <i>Enabled</i> , some POST tasks will be skipped to speed-up the BIOS boot process.
Quiet Boot	Disabled Enabled	<i>Disabled</i> displays normal POST diagnostic messages. <i>Enabled</i> displays OEM logo instead of POST messages. <i>Note: The default OEM logo is a dark screen.</i>
Boot Display	Clear Maintain	Controls the end of POST boot display handling, if Quiet Boot is enabled. If set to <i>Maintain</i> the BIOS will maintain the current display contents and graphics video mode used for POST display. If set to <i>Clear</i> the BIOS will clear the screen and switch to VGA text mode at end of POST. <i>Note: This option is only available if Quiet Boot is set to Enabled.</i>
Automatic Boot List Retry	Disabled Enabled	Automatically retry boot list if end of list is reached and no boot device found.
AddOn ROM Display Mode	Force BIOS Keep current	Set display mode for Option ROM.
Halt On Error	Disabled Enabled	Determines whether the BIOS halts and displays an error message if an error occurs. If set to <i>Enabled</i> the BIOS waits for user input.
Hit 'DEL' Message Display	Disabled Enabled	Allows/Prevents the BIOS to display the ' <i>Hit Del to enter Setup</i> ' message.
Interrupt 19 Capture	Disabled Enabled	Allows/Prevents the option ROMs (such as network controllers) from trapping the boot strap interrupt 19.
PXE Boot to LAN	Disabled Enabled	Disable/Enable PXE boot to LAN <i>Note: When set to 'Enabled', the system has to be rebooted in order for the Intel Boot Agent device to be visible in the Boot Device Priority Menu.</i>
Power Loss Control (see note below)	Remain Off Turn On Last State	Specifies the mode of operation if an AC power loss occurs. <i>Remain Off</i> keeps the power off until the power button is pressed. <i>Turn On</i> restores power to the computer. <i>Last State</i> restores the previous power state before power loss occurred. <i>Note: Only works with an ATX type power supply.</i>

Note

1. The term 'AC power loss' stands for the state when the module loses the standby voltage on the 5V_{SB} pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.
2. Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.
3. Unlike other module designs available in the embedded market, a CMOS battery is not required by congatec modules to support the 'Power Loss Control' feature.

9.6 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

9.6.1 Security Settings

Feature	Options	Description
Supervisor Password	Installed Not Installed	Reports if there is a supervisor password set.
User Password	Installed Not Installed	Reports if there is a user password set.
Change Supervisor Password	enter password	Specifies the supervisor password.
User Access Level	No Access View Only Limited Full Access	Sets BIOS setup utility access rights for user level.
Change User Password	enter password	Specifies the user password.
Password Check	Setup Always	Setup: Check password while invoking setup. Always: Check password also on each boot.
Boot Sector Virus Protection	Disabled Enabled	Select <i>Enabled</i> to enable boot sector protection. The BIOS displays a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. If enabled, the following appears when a write is attempted to the boot sector. You may have to type N several times to prevent the boot sector write. <i>Boot Sector Write!</i> <i>Possible VIRUS: Continue (Y/N)?</i> The following appears after any attempt to format any cylinder, head or sector of any hard disk drive via the BIOS INT13 hard disk drive service: <i>Format!!!</i> <i>Possible VIRUS: Continue (Y/N)?</i>
BIOS Update & Write Protection	Disabled Enabled	Only visible if a supervisor password is installed. If enabled the BIOS update and modification utilities will ask for the supervisor password before allowing any write accesses to the BIOS flash part.
END-Key Loads CMOS Defaults	Yes No	If set to Yes, the user can force the loading of CMOS defaults by pressing the END key during POST.

9.6.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently, however the drive will only lock if a user password is installed.

9.6.2.1 Hard Disk Security User Password

Feature	Options	Description
Primary/Secondary Master/Slave HDD User Password	enter password	Set or clear the user password for the hard disk. <i>Note: This option will be shaded if the hard drive does support the Security Mode Feature set but user failed to unlock the drive during BIOS POST.</i>

9.6.2.2 Hard Disk Security User Password

Feature	Options	Description
Primary/Secondary Master/Slave HDD Master Password	enter password	Set or clear the master password for the hard disk. <i>Note: This option will be shaded if the hard drive does support the Security Mode Feature set but user failed to unlock the drive during BIOS POST.</i>

9.7 Power Setup

Select the Power tab from the setup menu to enter the Power Management setup screen.

Feature	Options	Description
Power Management / APM	Disabled Enabled	Set this option to allow or prevent chipset power management and APM (Advanced Power Management).
Video Power Down Mode	Disabled Standby Suspend	Specifies the power state that the video subsystem enters when the BIOS places it in a power saving state after the specified period of display inactivity has expired.
Hard Disk Power Down Mode	Disabled Standby Suspend	Specifies the power state that the hard disk drives enter after the specified period of hard drive inactivity has expired.
Standby Timeout	Disabled 1- 60 Min	Specifies the length of time of inactivity the system waits before it enters standby mode.
Suspend Timeout	Disabled 1- 60 Min	Specifies the length of time of inactivity the system waits before it enters suspend mode.
<Device>	Ignore Monitor	Determines whether the device activity is monitored by the power management timer or not.
Power Button Mode	On/Off Suspend	Specifies if the system enters suspend or soft off mode when the power button is pressed.
Resume on Ring	Disabled Enabled	Disable/Enable RI (pin 89 of X4 = GPE2) to generate a wake event.
Resume on PME#	Disabled Enabled	Disable/Enable the PCI bus signal PME to generate a wake event.
Resume on RTC Alarm	Disabled Enabled	Disable/Enable RTC to generate a wake event.
RTC Alarm Date (Days)	1..15..31, Every Day	Select Alarm date using [+] / [-] keys.
System Time	[hh:mm:ss]	Select Alarm time using [Enter], [Tab] or [Shift-Tab] to select a field and [+] and [-] to configure the time.

9.7.1 Exit Menu

Select the Exit tab from the setup menu to enter the Exit setup screen.

You can display an Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup and reboot so the new system configuration parameters can take effect.
Discard Changes and Exit	Exit setup without saving any changes made in the BIOS setup program.
Discard Changes	Discard changes without exiting setup. The option values presented when the computer was turned on are used.
Load CMOS Defaults	Load the CMOS defaults of all the setup options.

10 Additional BIOS Features

The conga-E852 uses a congatec/AMIBIOS that is stored in an onboard Flash Rom chip and can be updated using the congatec System Utility, which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as E852R1xx, where E852 is the congatec internal project name, R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number.

10.1 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about “Updating the BIOS” please refer to the user’s guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

10.2 BIOS Recovery

The “BIOS recovery” scenario is recommended for situations when the normal flash update fails and the user can no longer boot back to an OS to restore the system. The code that handles BIOS recovery resides in a section of the flash referred to as “boot block”.

For more information about “BIOS Recovery” please refer to application note AN6_BIOS_Recovery_1.x.pdf, which can be found on the congatec AG website at www.congatec.com.

10.2.1 BIOS Recovery via Storage Devices

In order to make a BIOS recovery from a floppy disk, CD-ROM (ISO9660) or USB floppy the BIOS file must be copied into the root directory of the storage device and renamed *AMIBOOT.ROM*.

For more information about “BIOS Recovery via Storage Devices” please refer to application note AN6_BIOS_Recovery_1.x, which can be found on the congatec AG website at www.congatec.com.

10.2.2 BIOS Recovery via Serial Port

The Serial Flash method allows for boot block recovery by loading a BIOS image via a serial port (COM1). This can be used by many headless embedded systems which rely on a serial port as a debug and utility console port. This feature is disabled by default. See setup node in the “BIOS Setup Program” section 9.4.11 “Remote Access Configuration Submenu”.

For more information about “BIOS Recovery via Serial Port” refer to application note AN6_BIOS_Recovery_1.x, which can be found on the congatec AG website at www.congatec.com.

10.3 Serial Port and Console Redirection

Serial Redirection allows video and keyboard redirection via a standard RS-232 serial port.

For more information about “Serial Port and Console Redirection” please refer to application note AN2_Remote_Control_1.x.pdf, which can be found on the congatec AG website at www.congatec.com.

10.4 BIOS Security Features

The BIOS provides both a supervisor and user password. If you use both passwords, the supervisor password must be set first. The system can be configured so that all users must enter a password every time the system boots or when setup is executed.

The two passwords activate two different levels of security. If you select password support you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed.

The supervisor password (supervisor mode) gives unrestricted access to view and change all the setup options. The user password (user mode) gives restricted access to view and change setup options.

If only the supervisor password is set, pressing <Enter> at the password prompt of the BIOS setup program allows the user restricted access to setup.

Setting the password check to 'Always' restricts who can boot the system. The password prompt will be displayed before the system attempts to load the operating system. If only the supervisor password is set, pressing <Enter> at the password prompt allows the user to boot the system.

10.5 Hard Disk Security Features

Hard Disk Security uses the Security Mode feature commands defined in the ATA specification. This functionality allows users to protect data using drive-level passwords. The passwords are kept within the drive, so data is protected even if the drive is moved to another computer system.

The BIOS provides the ability to 'lock' and 'unlock' drives using the security password. A 'locked' drive will be detected by the system, but no data can be accessed. Accessing data on a 'locked' drive requires the proper password to 'unlock' the disk.

The BIOS enables users to enable/disable hard disk security for each hard drive in setup. A master password is available if the user can not remember the user password. Both passwords can be set independently however the drive will only lock if a user password is installed. The max length of the passwords is 32 bytes.

During POST each hard drive is checked for security mode feature support. In case the drive supports the feature and it is locked, the BIOS prompts the user for the user password. If the user does not enter the correct user password within five attempts, the user is notified that the drive is locked and POST continues as normal. If the user enters the correct password, the drive is unlocked until the next reboot.

In order to ensure that the ATA security features are not compromised by viruses or malicious programs when the drive is typically unlocked, the BIOS disables the ATA security features at the end of POST to prevent their misuse. Without this protection it would be possible for viruses or malicious programs to set a password on a drive thereby blocking the user from accessing the data.

10.6 Setup Resource Conflict Prevention Feature

The BIOS dynamically checks for resources and only displays those that are free as options. This prevents end users from making selections that could possibly cause resource conflicts.

This applies to the following BIOS setup options:

- All legacy I/O devices, such as serial ports, parallel ports, floppy controllers,
- PS/ mouse
- IDE controllers in legacy mode
- IRQ Resource Exclusion
- PCI Interrupt Routing

As a result of the dynamic resource checking, it's highly likely that not all options will be visible to the end user.

11 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Specification	Link
Audio Codec '97 Component Specification, Version 2.3 (AC '97)	http://www.intel.com/design/chipsets/audio/
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
PCI Specification, Revision 2.2	http://www.pcisig.com/specifications
Serial ATA Specification, Revision 1.0a	http://www.serialata.org
Advanced Configuration and Power Interface Specification Revision 2.0c, August 25, 2003	http://www.acpi.info
Information Technology AT Attachment with Packet Interface -5 (ATA/ATAPI-5) Revision 3, February 29, 2000	http://www.t13.org